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ABSTRACT

These volumes are, respectively, the self-instructional student manual and the teacher manual that cover the fourth set of training topics in this course. Both contain identical information on the chroma signal reproduction circuit, including a block diagram of a chroma signal reproduction circuit and sections on the bandpass amplifier circuit, the color synchronization circuit, the chroma signal demodulation circuit, the color matrix and output circuit, and the chroma signal processing circuit by inductive coupling. Circuit diagrams and block diagrams are included. (CML)

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TV TROUBLE-SHOOTING MANUAL
VOLUMES 9-10

Part 4: Chroma-Signal Reproduction Circuit

Student and Instructor's Manuals

Asian and Pacific Skill Development Programme
Islamabad, Pakistan

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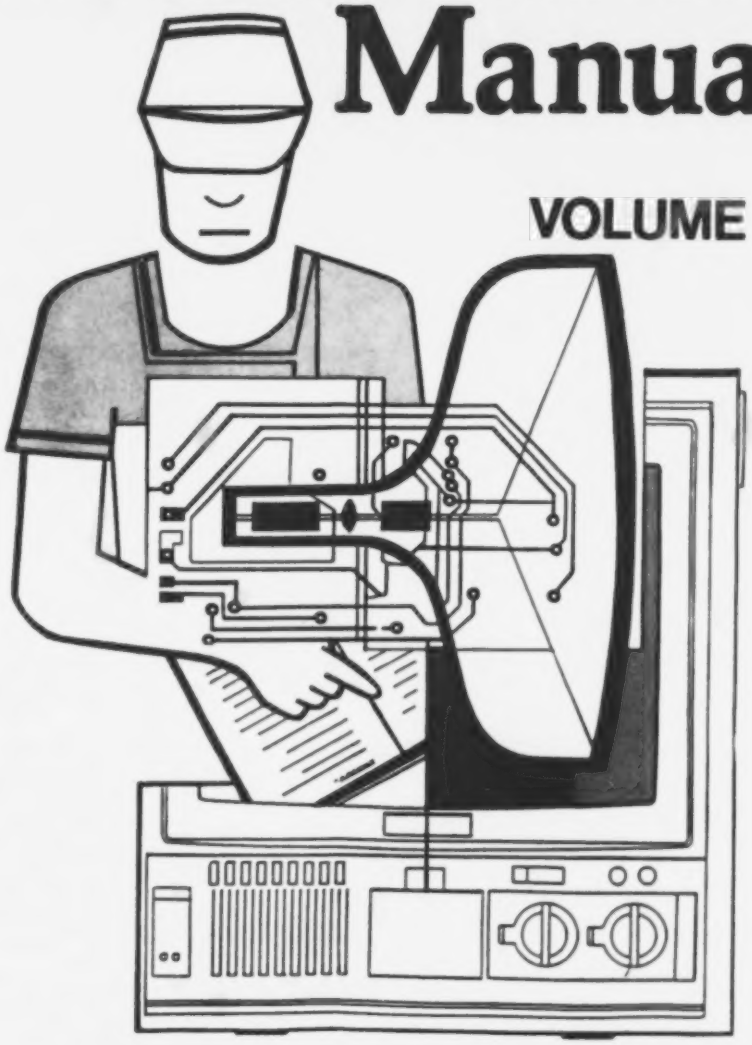
TV Trouble-shooting Manual

VOLUME



BY MASAAKI MUKAI AND RYOZO KOBAYASHI

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TV Trouble-shooting Manual

VOLUME 9

BY MASAAKI MUKAI AND RYOZO KOBAYASHI

Part 4: Chroma-signal reproduction circuit

ASIAN AND PACIFIC SKILL DEVELOPMENT PROGRAMME
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Part 4: Chroma-signal reproduction circuit

Block diagram of a chroma-signal reproduction circuit

Figure 4-1 shows block diagrams of three chroma-signal reproduction circuits, which are illustrated in three charts.

There are two types of video-detector circuits used in distinguishing the chroma signal from the composite video signal. One uses the same diode for detecting the luminance and chroma signals, as shown in Figures 4-1(a) and (b). The other type, shown in Figure 4-1(c), uses two diodes, one for detecting the luminance signal and the other for the chroma signal. The chroma signal is processed (or demodulated) further by either the colour-subtraction or the XZ demodulation circuit.

In the colour-subtraction demodulation circuit, either two or three colour-subtraction signals (ER-EY and EB-EY or ER-EY, EG-EY and EB-EY) are directly taken out from the output of the demodulation circuit, as shown in (a) and (c).

In the XZ demodulation circuit the EX and EZ signals are taken out. These signals are then matrixed by the succeeding stages to produce the R-Y, G-Y and B-Y signals, as shown in (b).

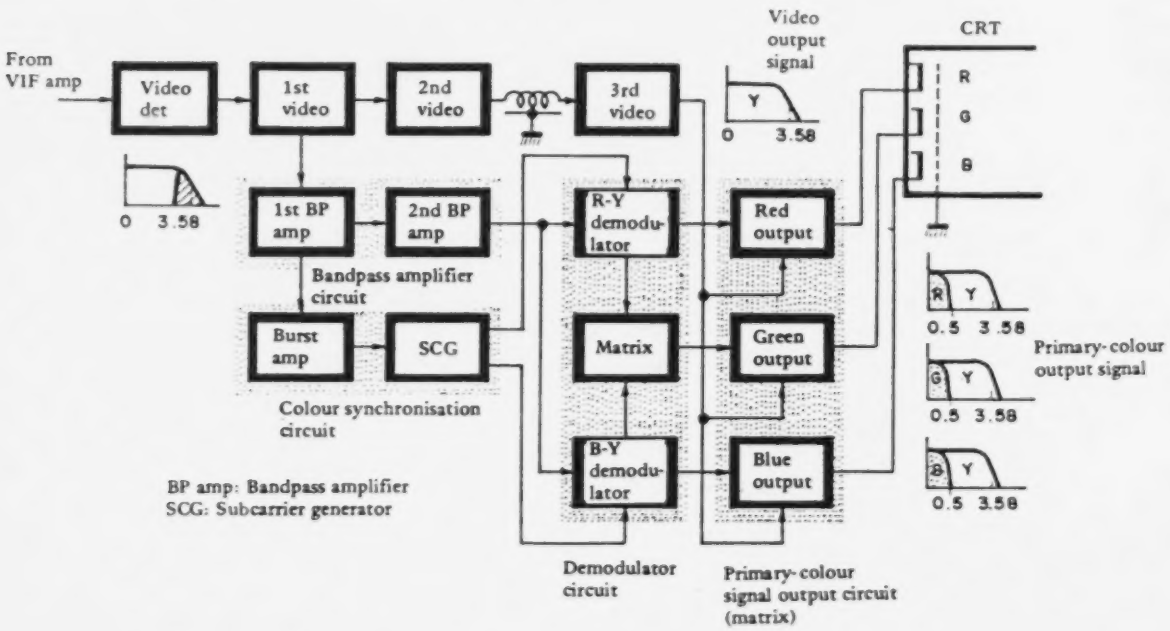


Figure 4-1(a)
Chroma-signal reproduction circuit
(Chroma and luminance signals are detected together, colour-subtraction demodulation and primary-colour circuit.)

With the introduction of colour demodulator circuits using an IC, the colour-subtraction demodulator circuit, with three primary-colour drive circuits, as shown in (a) and (c), is commonly used in modern colour receivers.

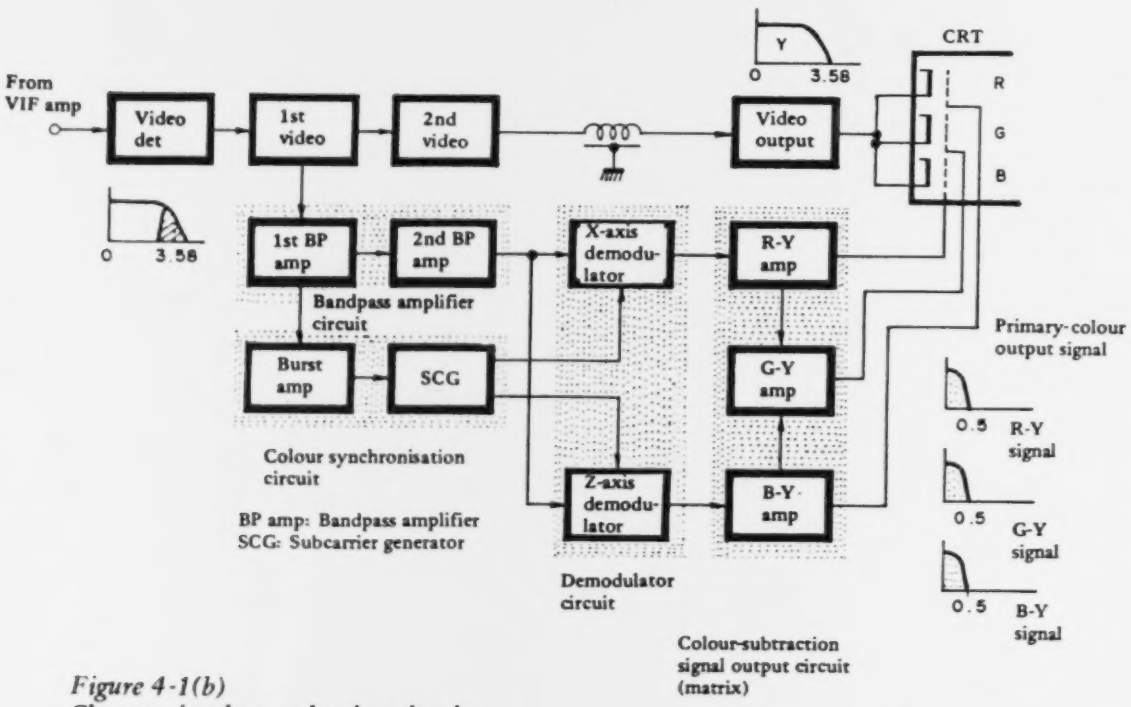


Figure 4-1(b)
Chroma-signal reproduction circuit
(Chroma and luminance signals are detected together, XZ-axis demodulation and colour-subtraction drive circuit.)

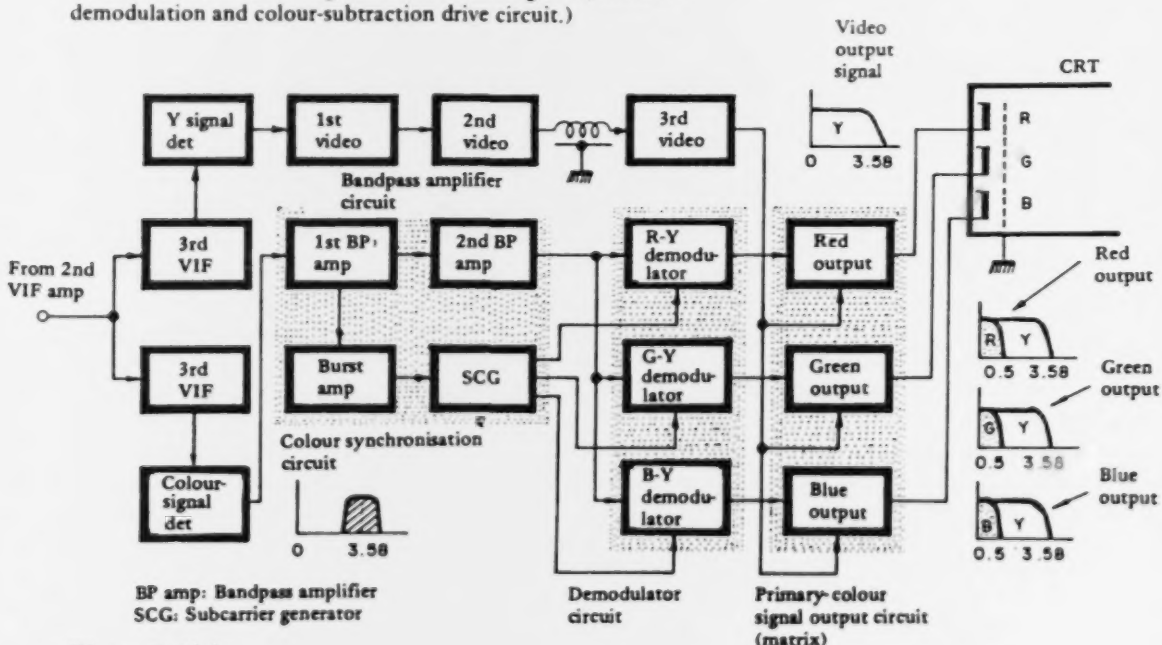


Figure 4-1(c)
Chroma-signal reproduction circuit
(Chroma and luminance signals are independently detected, colour-subtraction demodulation and primary-colour drive circuit.)

The bandpass amplifier circuit

Block diagram of a bandpass amplifier circuit and its functions

Figure 4-2 shows a functional block diagram of the bandpass amplifier circuit. This circuit amplifies the chroma signal and then supplies it to the chroma-signal demodulation circuit.

The bandpass amplifier circuit is tuned to 3.58 +/- 0.5 MHz. The following paragraphs discuss the detailed functions of this circuit.

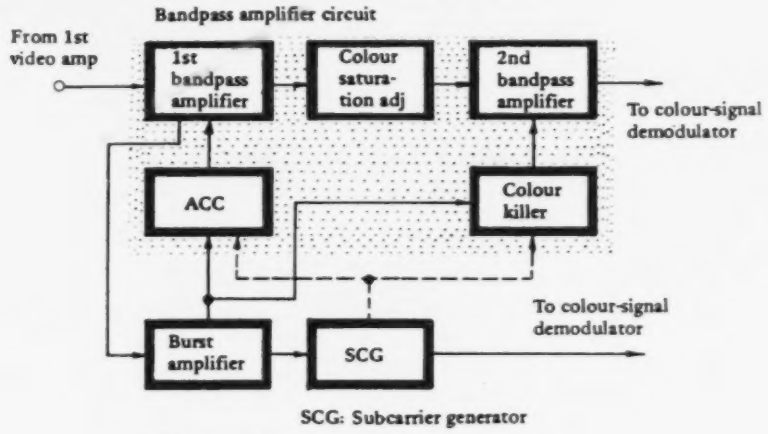


Figure 4-2
Functional block diagram of a bandpass amplifier circuit

It levels the amplitude of the chroma signal within the bandwidth. The chroma signal within the 0.5 MHz bandwidth must be symmetrical at 3.58 MHz, as shown in Figure 4-3(a). If it is not symmetrical, as shown in (b), proper colour reproduction cannot be obtained, because of the uneven frequency response of the chroma signal. However, the overall response of the chroma signal is not symmetrical, because it is located at the shoulder of the frequency spectrum of the composite video signal and is affected by the sound trap circuits.

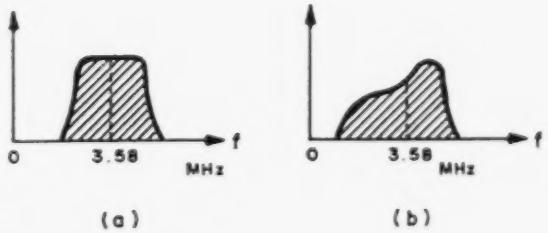


Figure 4-3
Chroma-signal frequency spectrum

As seen in the upper figure in 4-4(a) and (b), the higher components of the chroma signal are attenuated. The tuning circuit of the first bandpass amplifier circuit compensates the attenuation of the high-frequency components of the chroma signal to make the level or the strength of the sidebands of the chroma signal equal.

Figure 4-4 gives the signal flow in processing the chroma signal. Figure 4-4(a) gives the signal flow when the chroma and luminance signals are detected together; (b), the signal flow when these signals are detected independently.

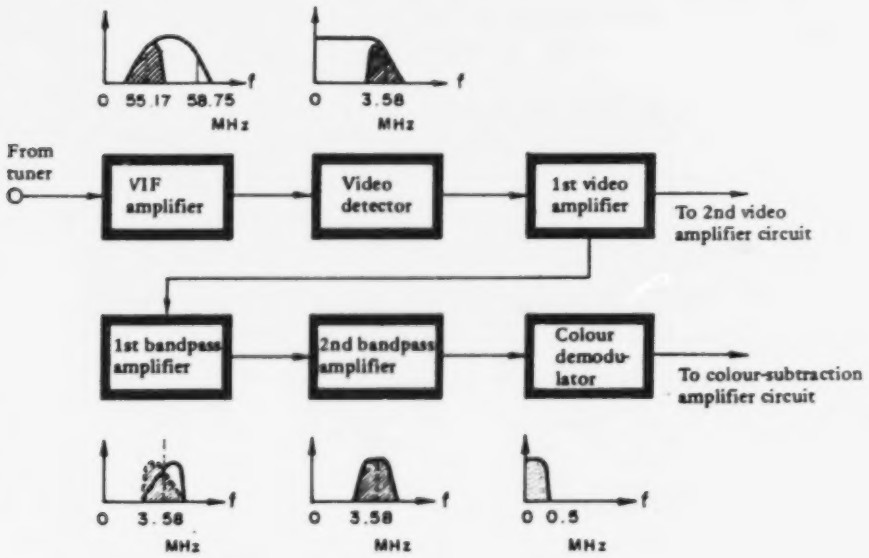


Figure 4-4(a)
Bandpass response
(Chroma and luminance signals are detected together.)

It controls colour saturation. The viewer should be able to adjust the colour saturation level according to his taste. The level can be varied by adjusting the gain of the bandpass amplifier circuit.

It has an automatic colour-control (ACC) circuit. An automatic level-control circuit called the ACC is used within the bandpass amplifier circuit. It maintains a chroma signal with a constant level despite variations in the TV signal strength or mismatch in the antenna to maintain a constant colour saturation level. This circuit uses the burst signals as a parameter.

Variations in the TV signal strength are detected by changes in the level of the burst signals, as shown in Figure 4-2. The ACC circuit either increases or decreases the gain of the bandpass amplifier circuit, depending on whether the strength of the burst signal decreases or increases.

It has a colour-killer circuit. When a black-and-white signal is received, the colour reproduction circuits should be disabled. Otherwise, the screen will be filled with colour noise or snow. The colour-killer circuit automatically disables the colour reproduction circuits when a monochrome signal is received.

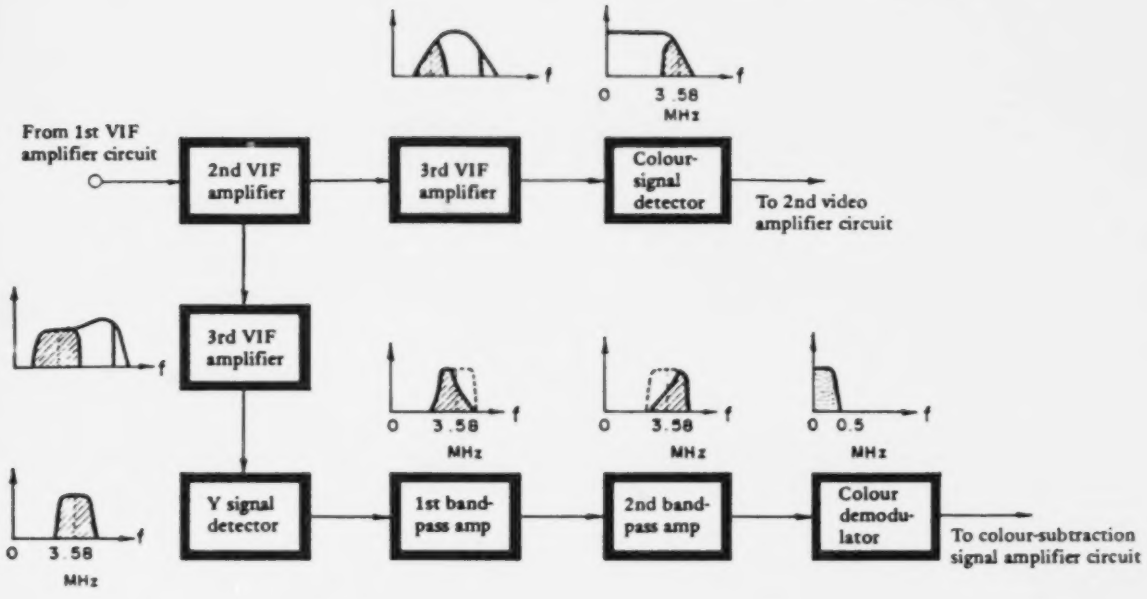


Figure 4-4(b)
Bandpass response
(Chroma and luminance signals are independently detected.)

It prevents the burst signals from penetrating the colour-demodulation circuit. The phase of the burst signals is used as the reference in determining the proper phase of the regenerated colour subcarrier signals for proper colour reproduction.

The colour burst signals are transmitted during the horizontal retrace periods to prevent them from interfering with the image on the screen. However, if the DC restoration of the colour-subtraction signal is done during the horizontal retrace period, the colour burst signals will affect the reference level of the restoration. To prevent this, one should disable the bandpass amplifier circuit during the horizontal retrace period.

First bandpass amplifier and ACC circuit

The burst signals are detected by the detector circuit in the ACC circuit. The ACC circuit produces a DC-control voltage proportional to the strength of the burst signal. The control voltage is used to control the gain of the first bandpass amplifier circuit.

ACC detector. There are three kinds of ACC detector circuits. Figure 4-5 shows examples of these circuits. Figure 4-5(a) is an example of a diode detector circuit.

The colour burst signals are amplified by the burst signal amplifier transistor Q3. The burst signals are coupled to the ACC detector diode D1 by C1. D1 conducts during the positive half-cycles of the burst signals.

The voltage across C1, whose polarity is shown in the figure, is called the ACC voltage. This voltage is supplied to the base of the ACC amplifier transistor Q2.

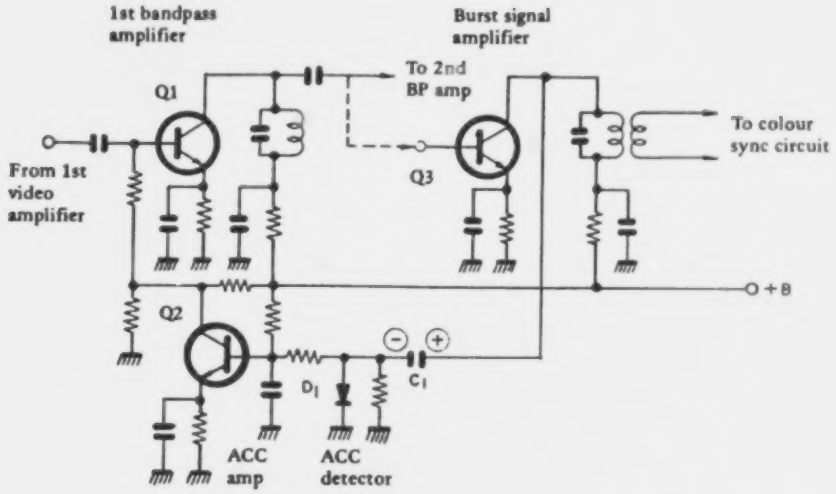


Figure 4-5(a)
Diode ACC detector circuit

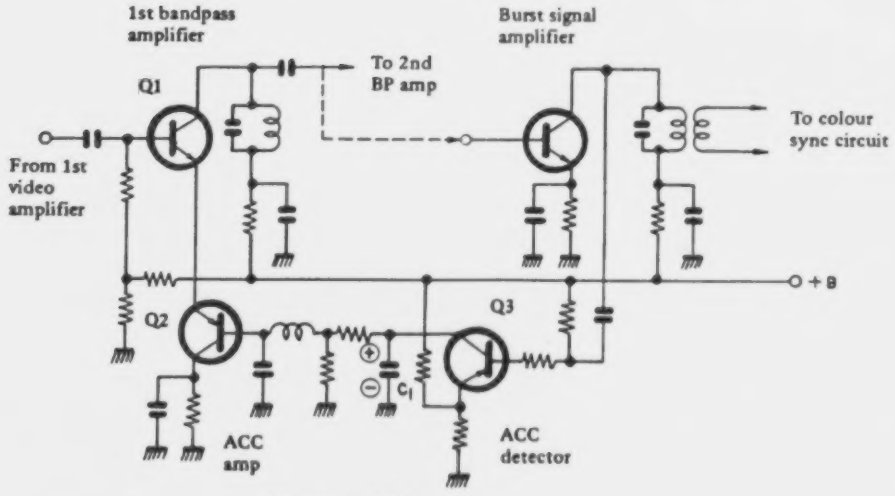


Figure 4-5(b)
Transistor ACC detector circuit

Figure 4-5(b) shows an ACC transistor-detector circuit. The burst signals are detected by the ACC detector transistor Q3. The burst signals are supplied to the base of Q3, and Q3 conducts during the negative half-cycles. The collector current of Q3 charges C1 and the voltage across it is called the ACC voltage.

Figure 4-5(c) shows an ACC phase-detector circuit. The colour burst and the colour subcarrier signals are supplied to the circuit.

The colour sync circuit synchronises the colour subcarrier frequency with the colour burst signal frequency.

The output voltage of the phase-detector circuit (taken at node [P]) is zero if the phase difference between the two signals is 90 degrees. The output becomes either positive maximum or negative maximum when the two signals are in phase (0 degrees apart) or 180 degrees apart, respectively.

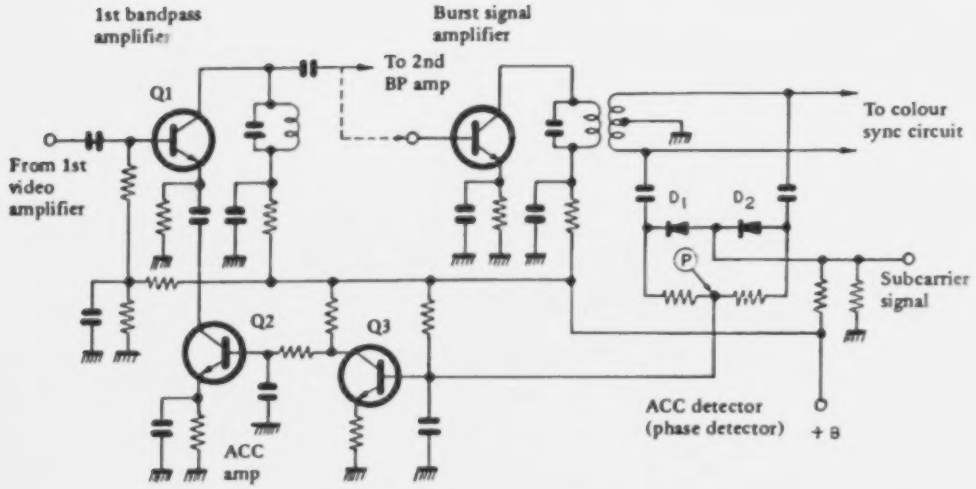


Figure 4-5(c)
ACC detector circuit by phase detector

However, the two signals supplied to the circuit are designed to have the same phase. Thus the output voltage is positive and its magnitude is proportional to the amplitude of the colour burst signals.

Besides detecting ACC, the circuit can determine the presence of the burst signals. Thus it is also used for the colour-killer circuit.

Gain control of the first bandpass amplifier circuit. There are three different circuits that can be used to control the gain of the bandpass amplifier circuit. All of them control the gain of the bandpass amplifier circuit if the amplitude of the colour burst signal changes.

In Figure 4-6(a) the gain of the first bandpass amplifier transistor (Q1) is controlled by varying its base voltage. The base voltage is varied by the ACC amplifier transistor Q2.

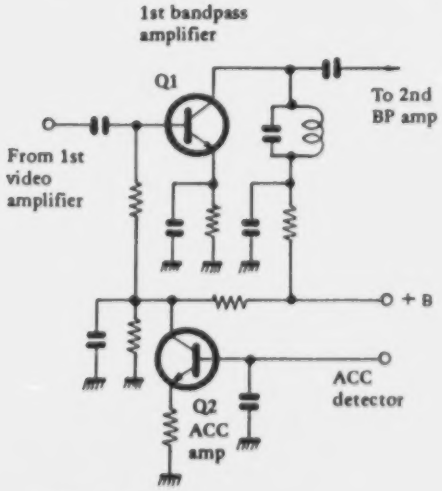


Figure 4-6(a)
Gain control by collector current

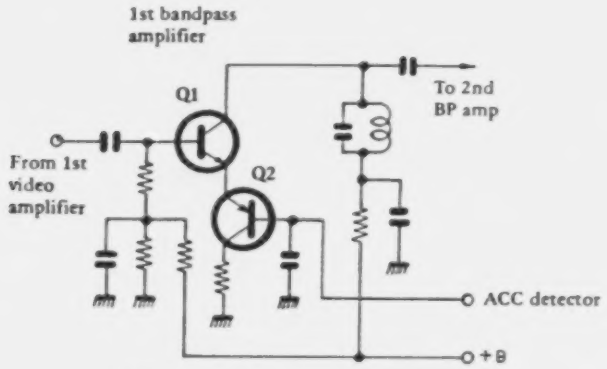


Figure 4-6(b)
Gain control by current feedback

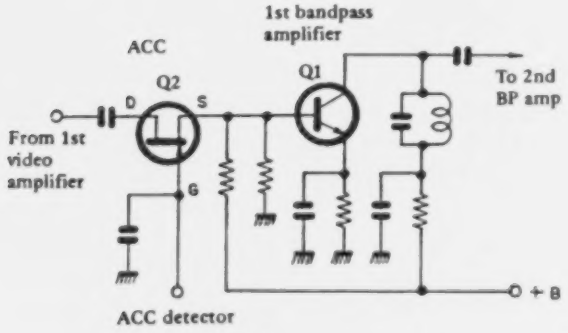


Figure 4-6(c)
Input signal control by a FET

In (b) the gain of the bandpass amplifier circuit is controlled by varying the amount of the emitter feedback of the bandpass amplifier transistor Q1. The amount of feedback to Q1 is varied by changing the internal resistance of Q2, which is connected to the emitter circuit of Q1. The internal resistance of Q2 can be controlled by the ACC voltage supplied to its base.

In (c) the amplitude of the output of the bandpass amplifier circuit is controlled by a FET. The FET is connected in series to the base circuit of the bandpass amplifier circuit.

The internal resistance of the FET is controlled by the ACC voltage. In turn, changes in the internal resistance of the FET are reflected as changes in the amplitude of the output of the first bandpass amplifier circuit.

Second bandpass amplifier and colour-killer circuit

The bandpass amplifier circuit must be disabled during black-and-white reception and enabled during colour reception. Colour reception is detected by checking the presence of the colour burst signals. The colour-killer circuit disables the colour-reproduction circuits during monochrome reception.

Figure 4-7 shows a colour-killer circuit. In Figure 4-7(a) a diode is used as the burst signal detector. A reverse bias voltage is supplied to the base-emitter junction of the second bandpass amplifier transistor Q1. Thus Q1 is normally cut off. If the burst signals are present, D1 conducts during the positive half-cycles and C1 is charged. The stored voltage across C1 turns on Q2.

When Q2 conducts, the base voltage of Q1 increases and turns on Q1. Without the burst signals the second bandpass amplifier transistor Q1 remains cut off.

Figure 4-7(b) shows a colour-killer circuit using a transistor detector.

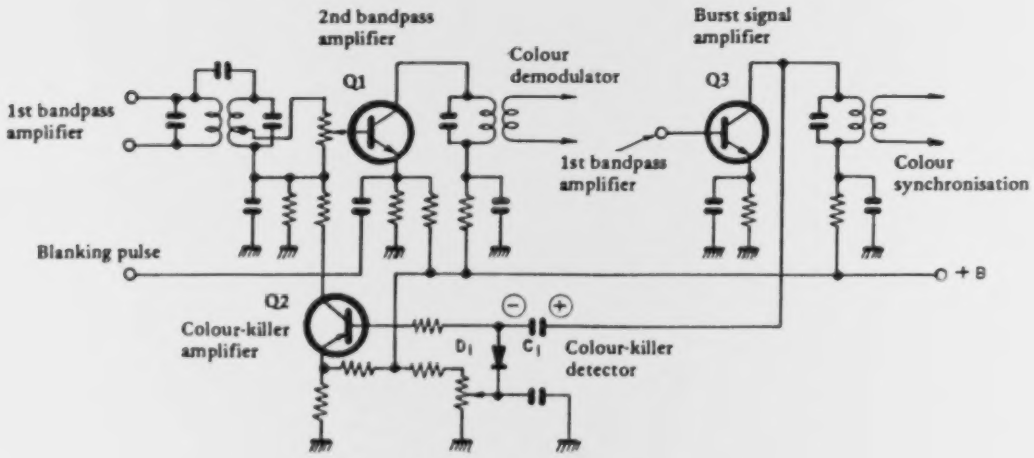


Figure 4-7(a)
Colour-killer circuit by a diode

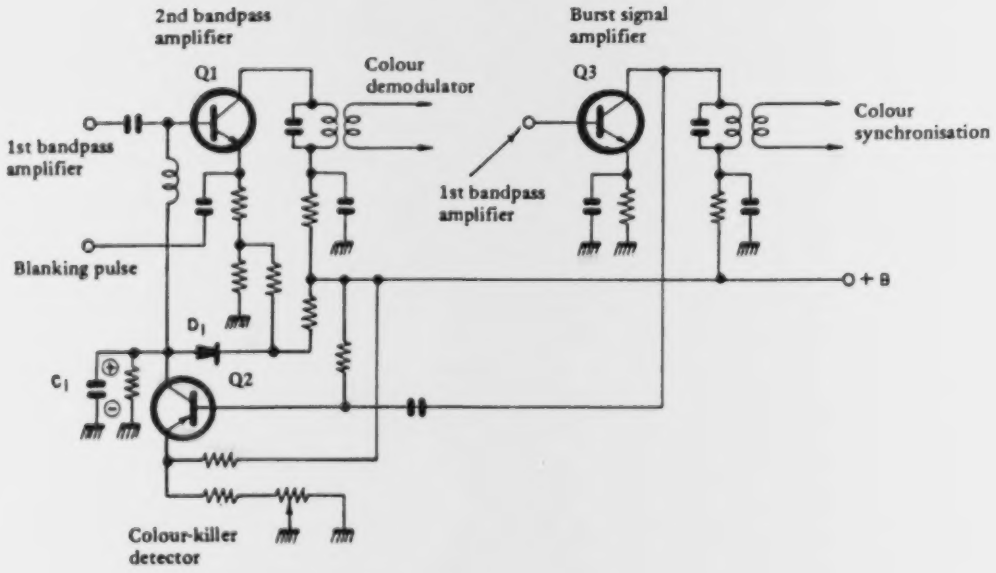


Figure 4-7(b)
Colour-killer circuit by a transistor

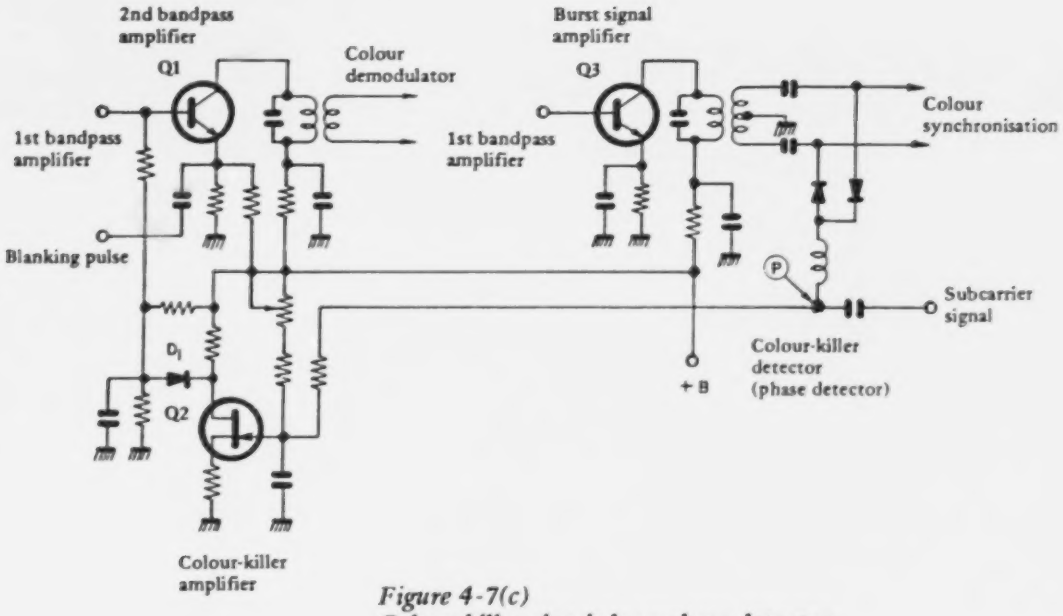


Figure 4-7(c)
Colour-killer circuit by a phase detector

If burst signals are present, the detector transistor Q2 conducts during the negative half-cycles and C1 is charged. The stored charge or voltage across C1 will trigger the second bandpass amplifier transistor Q1. Thus when the burst signals are present, the bandpass amplifier is enabled.

The diode (D1) connected to the collector of Q2 is a clamping diode. It conducts when the voltage across C1 exceeds a predetermined value and prevents Q1 from saturating.

Figure 4-7(c) is a colour-killer circuit using a phase-detector circuit.

A FET is used to control the second bandpass amplifier circuit. The phase-detector circuit operates like the ACC phase-detector circuit.

The output voltage of the detector (taken at node [P]) decreases when the burst signal is present. The output voltage is supplied to the gate of an N-channel FET (Q2). The drain current of this type of FET decreases when the gate voltage decreases.

When the burst signal is present, the gate voltage as well as the drain current of Q2 decreases. When the drain current of Q2 decreases, the drain voltage increases, and this turns on the second bandpass amplifier transistor Q1.

When the burst signals are absent, the second bandpass amplifier remains cut off. Thus the bandpass amplifier circuit is disabled during monochrome transmission and is enabled during colour transmission.

The diode (D1) connected to the drain circuit of the FET (Q2) conducts when the drain voltage of the FET becomes low and it firmly disables the second bandpass amplifier transistor.

The blanking pulses are supplied to the emitter circuit of Q1 in the circuits shown in (a), (b) and (c). These pulses disable the second bandpass amplifier circuit during the horizontal retrace periods to prevent the burst signals from affecting the DC restoration of the colour-subtraction signal.

Colour synchronisation circuit

Function of colour synchronisation circuit

Figure 4-8 shows a functional block diagram of the colour sync circuit. The main function of the colour sync circuit is to produce subcarrier signals needed in demodulating the colour signal.

The colour sync circuit uses the burst signals superimposed on the back porch of every horizontal blanking pulse to generate the subcarrier signal. A crystal with a frequency of 3.579545 MHz is used to produce a steady oscillation of the subcarrier signal.

The other functions of the chroma sync circuit are discussed in the following paragraphs.

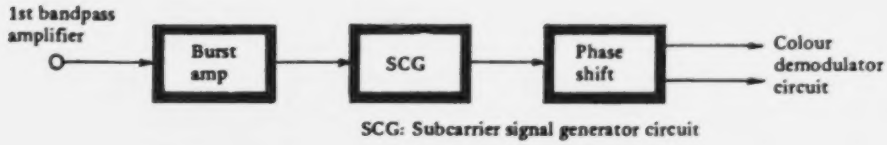


Figure 4-8
Functional block diagram of a colour sync circuit

Variable hue adjustment. The colour hue, or tint, of the image should be variable to allow the viewer to adjust the tint. The hue can be controlled by changing the phase between the subcarrier and the chroma signals. There are two ways of changing the phase relation of the chroma and subcarrier signals. One is to vary the phase of the chroma signal while keeping the phase of the subcarrier fixed. The other is to vary the phase of the subcarrier signal while keeping the phase of the chroma signal fixed. In the latter case, the phase of the subcarrier signal must be controlled within the colour sync circuit.

Generation of two or three subcarrier signals. The two-axis colour demodulator circuit requires two kinds of subcarrier signals while the three-axis colour demodulator circuit requires three to demodulate the chroma signal.

The phase of the subcarrier signals must meet the requirements of the demodulator circuit. A phase-shift circuit is used to shift the phase of the subcarrier signals to meet the phase requirements of the colour demodulator circuit.

Burst signal amplifier circuit

The chroma signal amplified by the first bandpass amplifier circuit is supplied to the burst amplifier circuit. Then the burst signal amplifier circuit separates the burst signals from the chroma signal and amplifies them.

Figure 4-9 shows examples of burst signal amplifier circuits. In the circuit shown in (a), positive flyback pulses from the horizontal output transformer

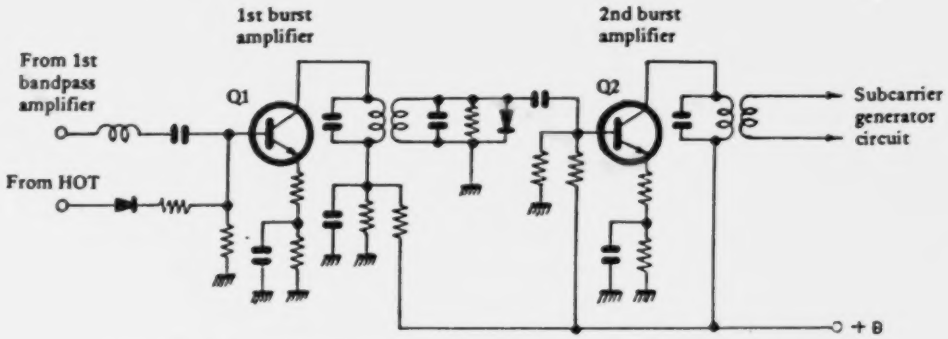
(HOT) are supplied to the burst signal amplifier transistor Q1, which is biased in cut-off. These pulses trigger the transistor on during the horizontal retrace periods.

Since only the burst signals are present during the retrace periods, the burst signals are separated from the chroma signal and amplified.

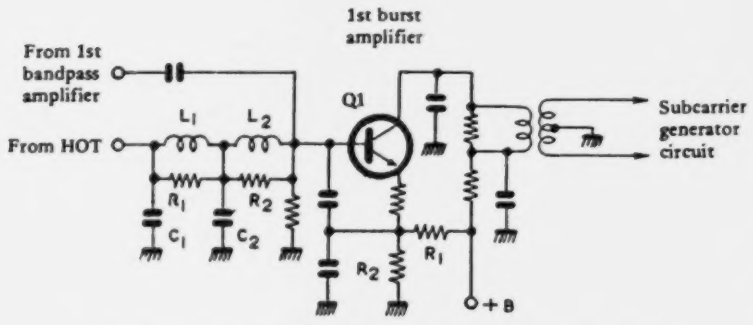
Figure 4-9(b) shows another example of a burst signal amplifier circuit. Positive horizontal sync signals are supplied to the base of the burst signal amplifier transistor Q1. These signals are used for triggering Q1. However, the burst signals are located on the back porch of every horizontal blanking signal. Thus the horizontal sync signal has to be delayed in order to trigger Q1 on during the burst signal periods. The delay circuit is formed by C1, C2, L1, L2, R1 and R2.

Subcarrier signal generator circuit

Figure 4-10 shows block diagrams of subcarrier generator circuits. There are three types of subcarrier signal generator circuits: 1) crystal filter (ringing type), 2) burst signal injection lock and 3) APC (automatic phase control). All these circuits use a crystal for a stable oscillation.



(a) Burst signal amplifier circuit using pulses from horizontal amplifier circuit



(b) Burst signal amplifier circuit using synchronising pulses

Figure 4-9
Burst signal amplifier circuits

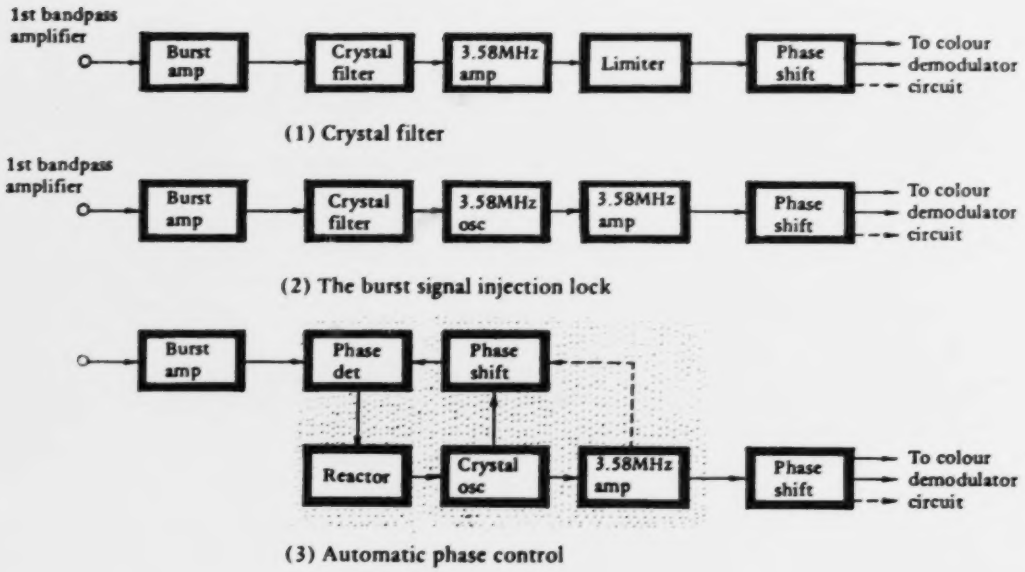


Figure 4-10
Subcarrier signal generator circuit

Crystal oscillator. When pressure or tension is applied across a thin piece of crystal, electricity is generated at the surface.

A crystal can be made to oscillate by applying an AC voltage across the crystal through electrode plates attached at opposite surfaces of a thin piece of crystal. The oscillation of the crystal is stable and is not affected by temperature changes.

A crystal can be used in an electrical circuit for a steady and constant oscillation in an oscillator or filter circuit.

In Figure 4-11(a) if the magnitude of the RF voltage applied to the crystal is kept constant while the frequency is varied, the relation between the frequency of the applied voltage and the current through the crystal is shown in (c).

In (c) the frequency at which maximum current flows is called the series resonant frequency (fs), and the frequency at which minimum current flows is called the parallel resonant frequency (fp). The difference between fs and fp is very small; thus the curve at (c) can be approximated by the curve at (d).

Picture 4-1
Crystals used as oscillators in TV receivers

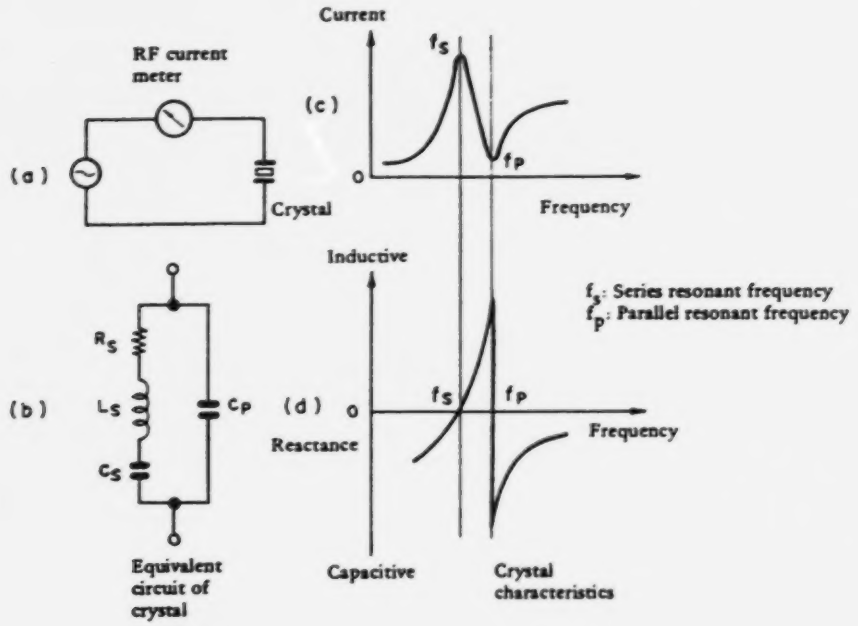


Figure 4-11
Equivalent circuit and characteristic of a crystal

The series and parallel resonance characteristic of the crystal makes it a mechanical oscillator.

Figure 4-11(b) is an equivalent circuit of a crystal. Rs, Ls and Cs are the equivalent series impedances of the crystal; Cp is the equivalent capacitance across the crystal due to the electrodes.

Picture 4-1 shows crystals used as oscillators in TV receivers.

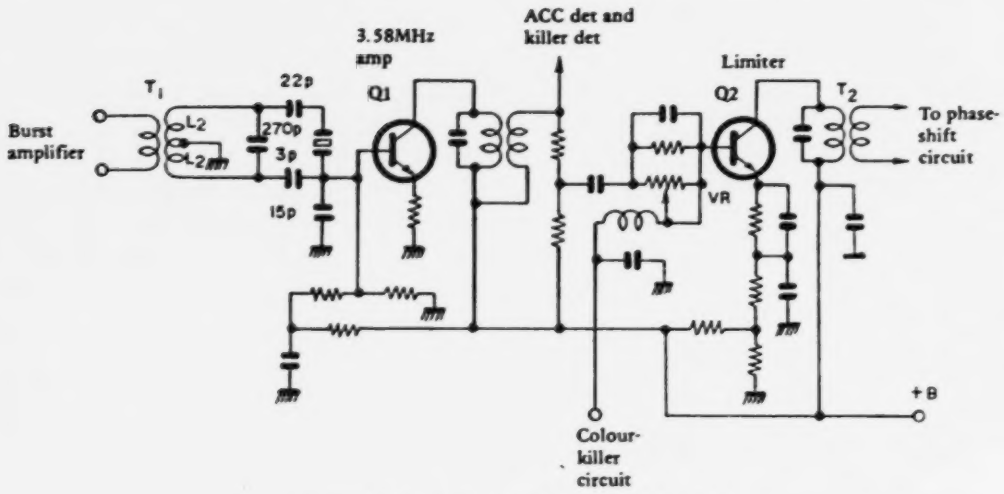
Crystal-filter (ringing type) oscillator. Figure 4-12(a) shows a subcarrier generator circuit using a crystal-filter circuit. The burst signals are coupled by Q1 to the crystal-filter circuit. The filter circuit converts the burst signals into a continuous signal. The amplitude of the continuous signal is made constant by an amplitude limiter circuit to produce a subcarrier signal.

Figure 4-13(a) shows the stages in transforming the burst signals into a colour subcarrier signal. The function of the crystal-filter circuit is explained in Figures 4-12(b) and (c). In Figures 4-12(b) and (c) the burst signals are supplied to L1 and L2 through terminals A and B. The output of the circuit is taken across terminals C and D.

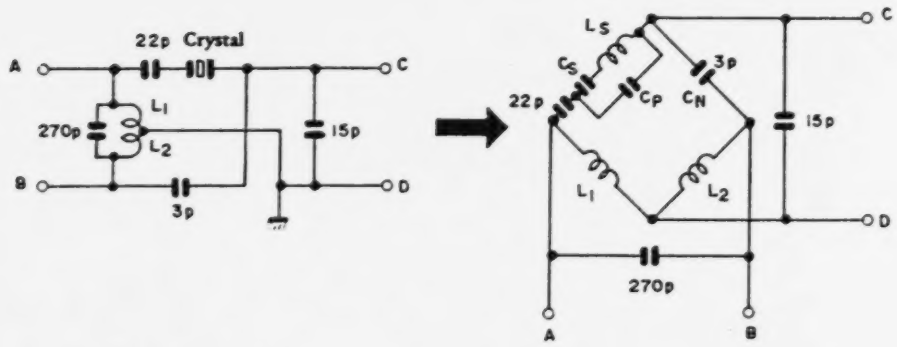
Figure 4-12(c) shows a bridge-circuit equivalent of (b). This circuit is balanced at frequencies other than the resonant frequency of the crystal filter. For a balanced bridge circuit, the formula below is satisfied.

$$CP/CN = L1 / L2$$

When the bridge circuit is balanced, the output is zero. Thus when the frequencies of input signals and noise are unequal to the resonant frequency (fs), the output signal is zero. The crystal used in this circuit is a 3.579545 MHz crystal.



(a) Crystal-filter circuit used in an actual circuit



(b) Crystal-filter circuit

(c) Equivalent circuit

Figure 4-12
Crystal-filter circuits

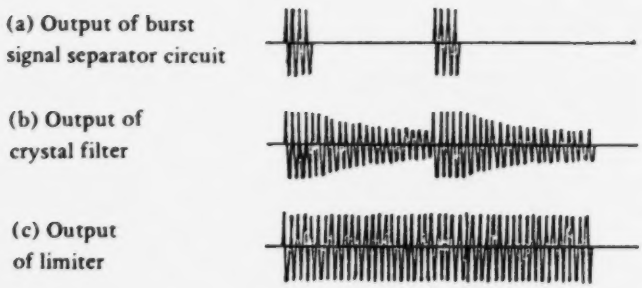


Figure 4-13
Wave-form analysis of crystal-filter circuit

When the burst signals are supplied to terminals A and B, the circuit becomes unbalanced and a continuous signal with frequency equal to the burst signal frequency is taken across C and D. Thus this filter circuit prevents interference of external signals.

The variable resistor VR in Figure 4-12(a) is for the hue adjustment. The phase of the subcarrier signal is varied by around +/-30 degrees by changing the input static capacitance of the limiter transistor Q2 through the adjustment of VR. Q2 is disabled by the colour-killer circuit during black-and-white reception.

Burst signal injection lock. Figure 4-14 shows a burst signal injection lock circuit. In the figure, the 3.58 MHz oscillator circuit is autodyned and uses no crystal oscillator to generate the subcarrier signal. Instead it is fed an accurate 3.58 MHz signal taken from the output of the crystal filter circuit. The output of the crystal filter synchronises the oscillation frequency of the 3.58 MHz oscillator circuit with the burst signals.

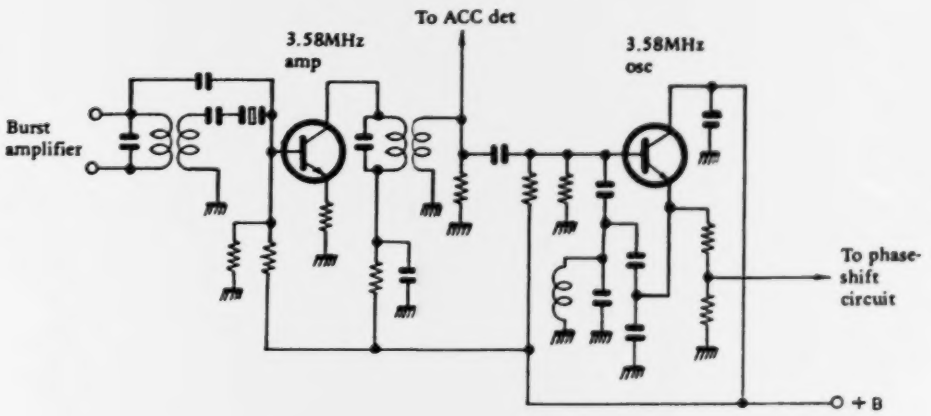


Figure 4-14
A burst signal injection lock circuit

Automatic phase control (APC). The principle of this circuit is entirely different from the subcarrier generators. A block diagram of the circuit is shown in Figure 4-10(c). The circuit compares the phase of burst signals and the 3.58 MHz oscillator signal and produces a subcarrier signal synchronised with the burst signals.

Figure 4-15 shows an APC circuit. The burst signals and the output of the 3.58 MHz crystal oscillator signal (actually horizontal output pulses) are supplied to the phase-detector circuit. This circuit detects any phase difference between the two signals and produces a control voltage which is taken out at node (P). The control voltage is supplied to the oscillator circuit and varies the voltage across the varicap diode connected in series to the crystal.

The phase and frequency of the oscillator signal are controlled by the varicap and are synchronised with the burst signals.

Because it is reliable the APC subcarrier oscillator circuit is commonly used in colour IC TV receivers.

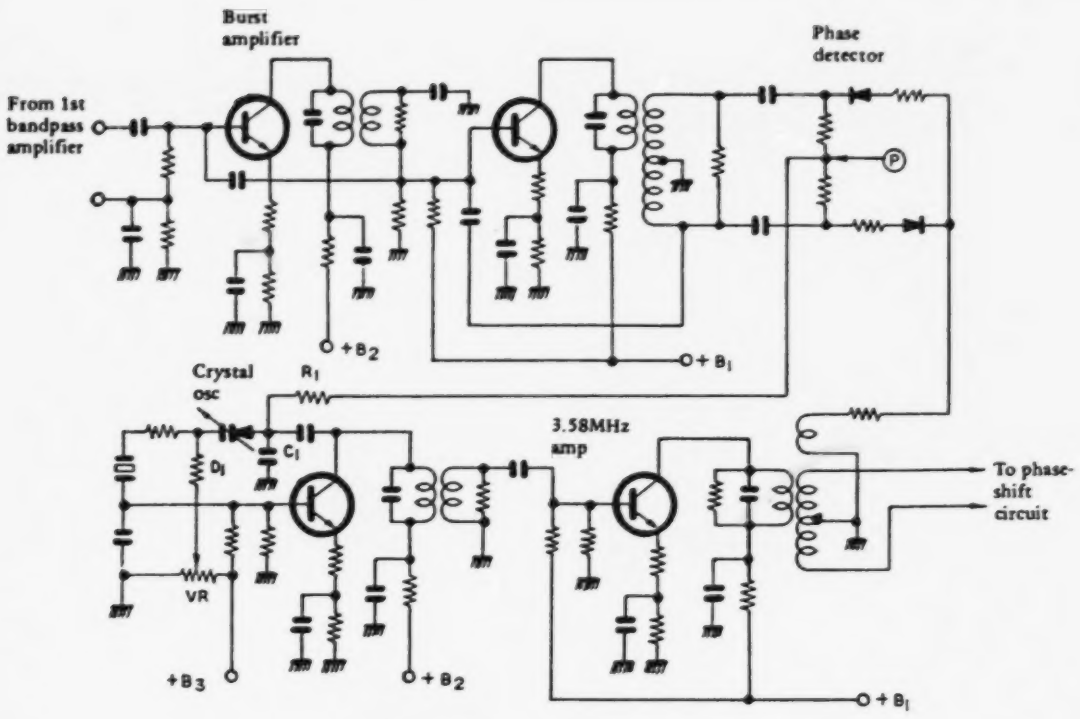


Figure 4-15
An APC circuit

Phase locked loop (PLL). This loop belongs to the APC type but uses no capacitors or inductors in the tuning circuit.

A functional block diagram of a PLL circuit is shown in Figure 4-16. It consists of a phase detector, low-pass filter and a voltage-control oscillator (VCO) circuit. The burst signals and the output of the VCO circuit are fed to the phase-detector circuit. The phase-detector circuit compares the phase of the two signals and produces a control voltage proportional to the difference. The control voltage is fed to the VCO circuit through a low-pass filter and synchronises the VCO output with the burst signals.

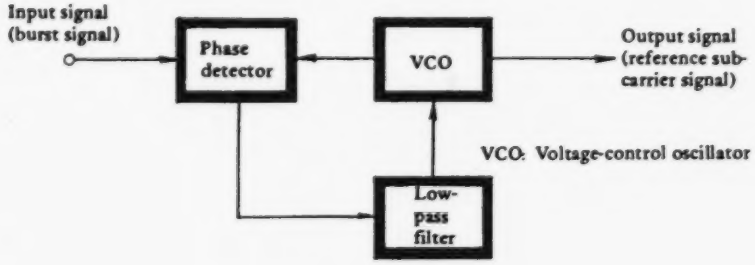
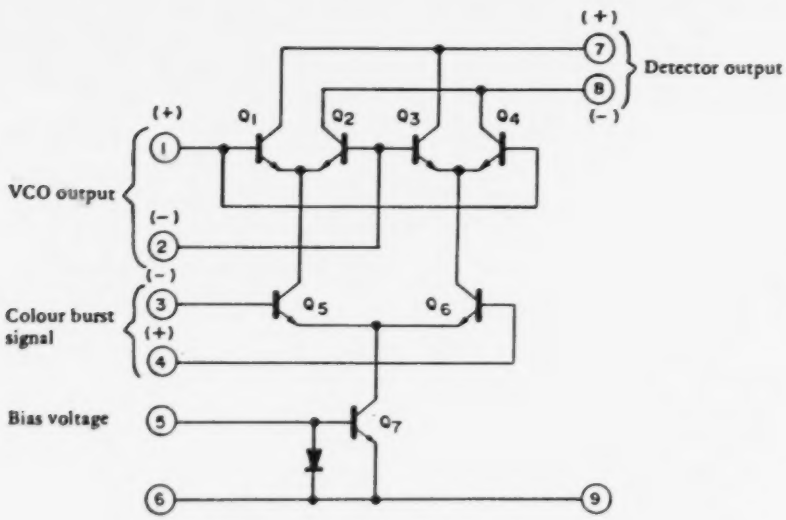


Figure 4-16
A PLL circuit

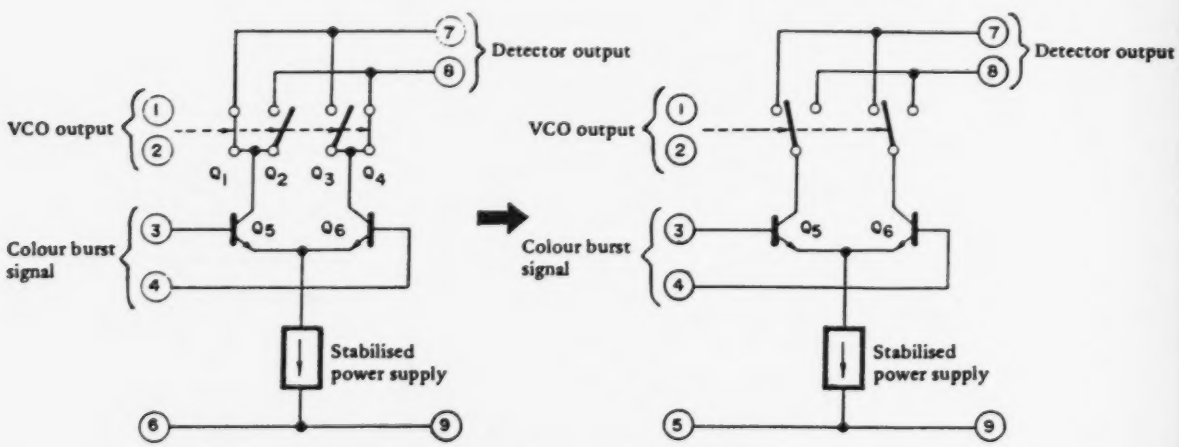
Phase-detector circuit. Figure 4-17(a) shows a phase-detector circuit. A differential amplifier circuit, dual-balanced, is usually used as a phase detector.

The output signal of the VCO is fed to the upper differential amplifiers through terminals (1) and (2); the burst signals are fed to the lower differential amplifier through terminals (3) and (4). The upper differential amplifiers formed by Q1 to Q4 merely function as a switch controlled by the VCO output, as shown in Figure 4-17(b). The lower differential amplifier increases the burst signals. The amplified burst signals are switched from terminals (7) to (8) alternately by the upper differential transistors.

The state of the switches (Q1 to Q4) depends on the cycle of the VCO output. The output of the phase detector depends on the phase relation between the VCO output signal and the burst signals.



(a) Cross collector coupling



(b) Switching of Q1, Q2, Q3, Q4 by VCO signals

Figure 4-17
A PLL phase-detector circuit

Figure 4-18 shows examples of the phase-detector output for three different phase relations between the VCO output and the burst signals. The examples given are for the cases when the burst signals and the VCO output are 0 degrees (in phase), 180 degrees (negative phase) and 90 degrees apart. When the burst and the VCO signals are 0 degrees and 180 degrees apart, the average phase-detector output is maximum. When the signals are 90 degrees apart, the output is zero.

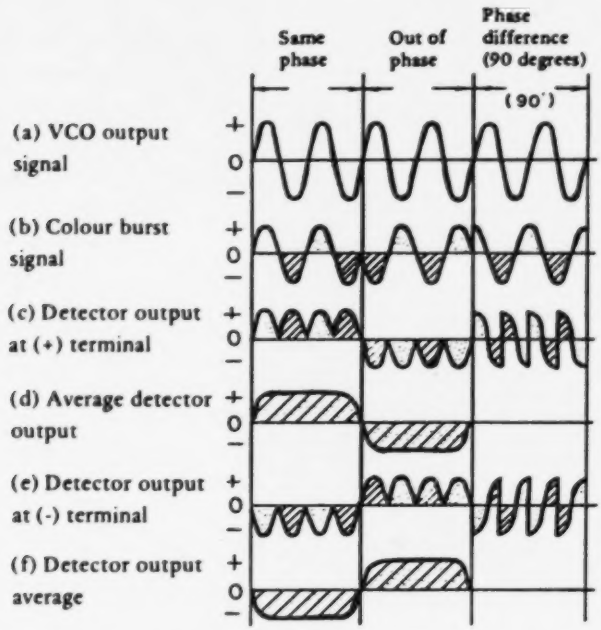


Figure 4-18
Phase relation and output voltage

VCO circuit. In inductive-coupling circuits it is impractical to use variable resistors and inductors to change the level and the phase of a signal, respectively. Instead the supply voltages of the transistors within the IC are varied to control the level and phase of the signals.

Since the function of the IC is controlled by the supply voltage, reactive interference from other circuits can be reduced. This kind of circuit control is called voltage control. It is also used in the frequency-control circuit of the 3.58 MHz oscillator circuit of the colour sync circuit. Figure 4-19 shows a functional block diagram of the VCO circuit.The oscillator frequency is controlled by the DC voltage supplied to the phase-shift circuit. This circuit changes the phase of the feedback circuit, thus maintaining the frequency of the oscillator. Figure 4-20 shows an actual VCO circuit.

Transistors Q1 to Q6 form dual-balanced differential amplifier circuits.

The output signals are independently taken out from the emitter circuits of Q7 and Q8 through R and C and then mixed together. After mixing, the output signals are fed back to the differential amplifier circuit through a crystal. The circuit works like a CR oscillator circuit.

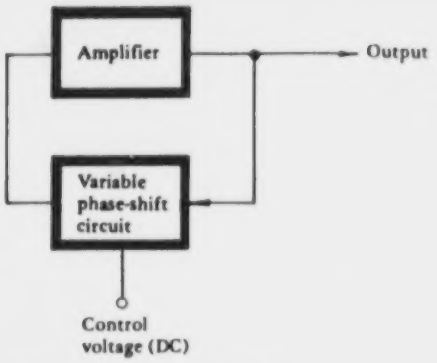


Figure 4-19
Functional block diagram of a VCO circuit

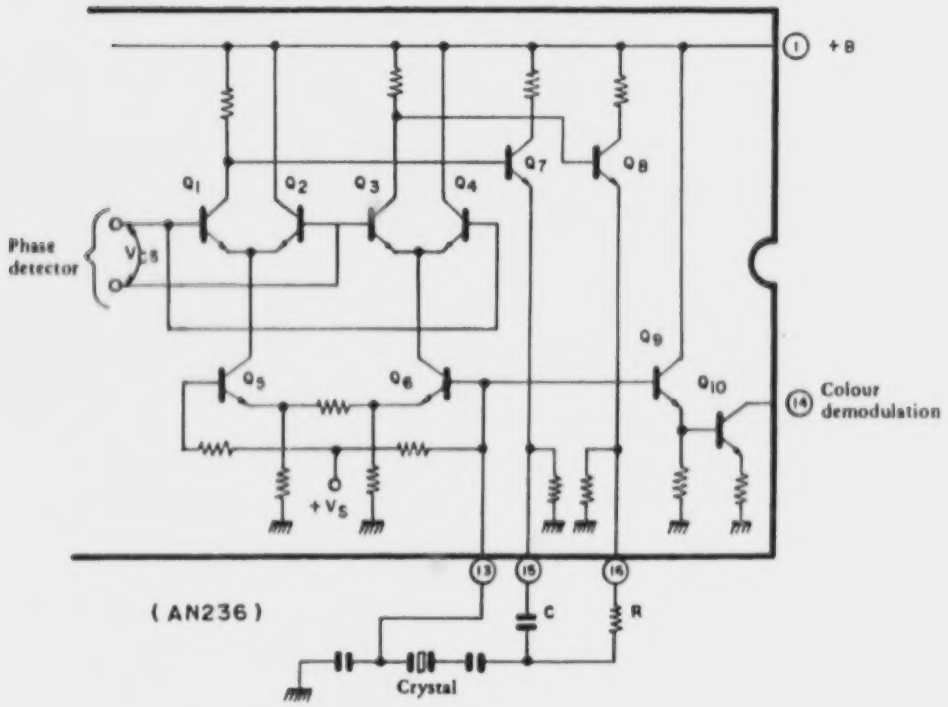


Figure 4-20
A VCO circuit

The DC voltage-control signal (Vcs) produced by the phase-detector circuit is supplied to the base of transistors Q1 to Q4. This DC voltage varies the operation of the transistors. Transistors Q1 to Q4 form pairs of differential amplifier circuits so when Q1 and Q4 conduct more, Q2 and Q3 conduct less.

If the output of Q1 increases, the signal through Q7 and C increases. On the other hand, Q3 conducts less and the signal through Q8 and R decreases. Thus the phase of the feedback signal in the feedback circuit of the VCO circuit advances (the oscillation frequency increases). Similarly, if the output of Q1 decreases, the signal through Q7 and C decreases and the signal through Q8 and R increases. This results in a lag in the phase of the feedback signal in the feedback circuit of the VCO circuit (oscillation frequency decreases). Therefore, by supplying a DC-control voltage to the base of Q1 to Q4, the phase of the feedback signal of the VCO circuit is varied, and so the oscillation frequency of the VCO circuit is maintained.

The chroma-signal demodulation circuit

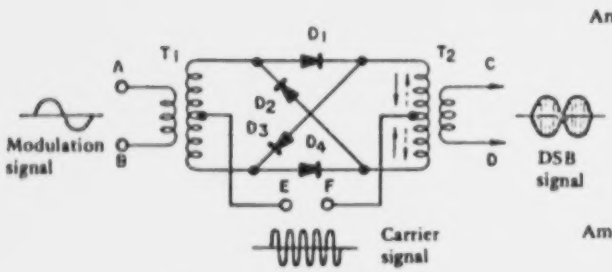
This circuit processes the chroma signal to produce the colour-subtraction signals.

Principle of demodulation

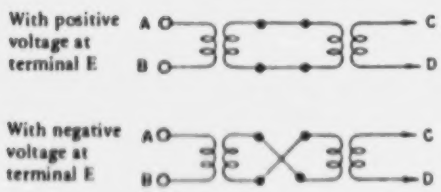
Generation of DSB (double sideband) signal. The chroma signal is an amplitude-modulated signal transmitted with its carrier suppressed at the transmitter.

The transmitter sends only the upper and lower sidebands. This is called double sideband transmission. Figure 4-21(a) shows a DSB generator circuit.

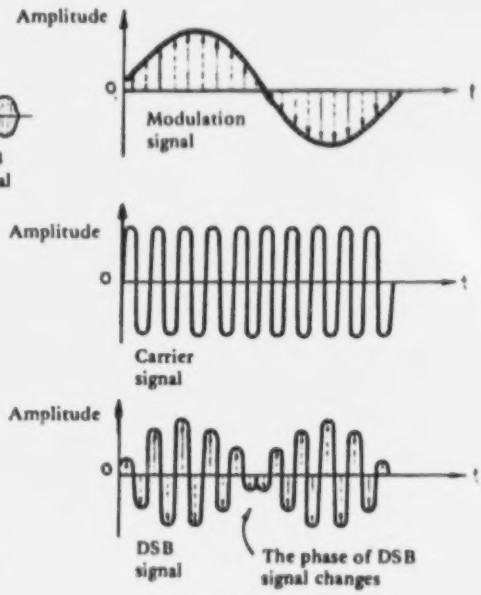
The modulating signal is supplied to terminals A and B; the carrier signal, to terminals E and F. The amplitude of the carrier signal is made greater than that of the modulating signal.



(a) DSB signal generator circuit



(b) Circuit response by the polarity of carrier signal



(c) DSB signals

Figure 4-21
Principle of DSB signal generator circuit

When the modulating signal alone is supplied. The signal induced at the secondary of the input transformer T1 by the modulating signal is shorted by diodes D1, D3 or D2, D4. The impedance of the output transformer T2 is much lower than the modulating signal, since the modulating signal has a frequency much lower than the frequency of the carrier signal. Thus no output is developed across terminals C and D.

When the carrier signal alone is supplied. The diodes are switched by the polarity of the carrier signal supplied to terminals E and F. When terminal E is positive and F is negative, diodes D1 and D4 are supplied with forward bias and conduct, while D2 and D3 are reverse-biased and cut off.

When the polarity of the terminals is reversed, the state of the diodes is also reversed. Thus D1D4 and D2D3 are alternately switched by the carrier signal in every half-cycle. The currents through the primary of the output transformer T2 are equal in magnitude and opposite in direction, as shown in Figure 4-21(a). Thus the currents cancel each other and no signal is produced across the output terminals C and D.

When the modulating and carrier signals are supplied together. In Figure 4-21 the diodes act as switches triggered by the carrier signal. Figure (b) shows how the circuit in (a) is switched by the carrier signal. As shown in (c) the modulated signal flows in opposite directions within the secondary of the output transformer T2 with respect to the cycle of the carrier signal.

The signal at the output (across terminals C and D) has no carrier component, but has a frequency equal to the carrier signal frequency. The amplitude of the output signal is proportional to the amplitude of the modulating signal. This signal is called a DSB (double sideband) signal. Figure 4-21(c) shows an example of a DSB signal.

The output is zero if the amplitude of the modulating signal is zero. The DSB signal at the output is in phase with the carrier signal during the positive cycle of the modulating signal and is in opposite phase with the carrier signal during the negative cycle.

Demodulating the DSB signal. The same circuit shown in Figure 4-21 is used to demodulate the DSB signal. The DSB signal is supplied to terminals A and B; the carrier signal, to terminals E and F. During demodulation the circuit operates the same way it does during modulation. Similarly the output is taken across terminals C and D.

The carrier signal supplied to terminals E and F for demodulating the DSB signal must be in phase and equal in frequency with the modulated carrier signal at the transmitter. In colour receivers the carrier signal needed to demodulate the DSB (chroma) signal is generated by the colour sync circuit. This signal is called the subcarrier signal.

Demodulating the chroma signal. The chroma signal is a mixture of two DSB signals, the ER-EY and EB-EY signal. The carrier of the ER-EY and EB-EY signals has the same frequency but with a phase difference of 90 degrees. Thus the two DSB signals (ER-EY and EB-EY) are also 90 degrees apart.

To prevent overmodulation, the ER-EY signal is modulated at a rate limit of 1/1.14; the EB-EY signal, at a rate limit of 1/2.03 at the transmitter.

Figure 4-22(a) shows the phase relation of these two signals. A complete cycle of the (1/1.14) (ER-EY) and (1/2.03) (EB-EY) modulating signals is given. Figure 4-22(b) shows the sum of the two signals. This is transmitted by the TV station as the chroma signal. Let us discuss the demodulation of the chroma signal shown in (b).

Assume the colour burst signal to be 180 degrees out of phase. By calculation using the equation of the curve in (b) or by graphic analysis, the magnitude of the demodulator output is 0.49 when the phase of the subcarrier signal (fs) is 0 degrees.

From (a) this magnitude corresponds to 1/2.03 times the EB-EY signal alone, since in this case the ER-EY component of the signal is zero. Thus when

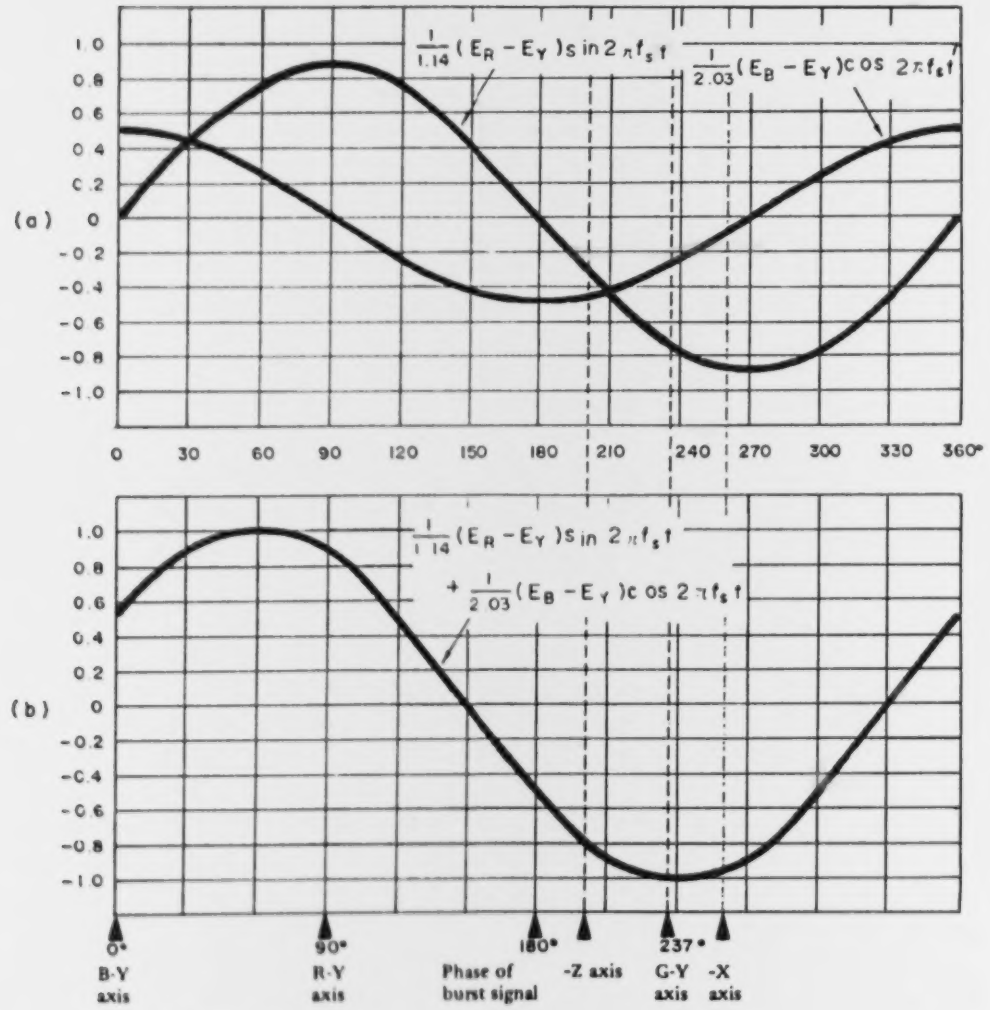


Figure 4-22
Phase shift of colour subcarrier signal and demodulation axis

the phase of the subcarrier signal is 0 degrees, the demodulator output consists only of the EB-EY signal. Similarly if the phase of the subcarrier signal is 90 degrees, the demodulator output consists only of the ER-EY signal.

As shown in (b), if the phase of the subcarrier is 237 degrees, the magnitude of the demodulator output is -0.99. From (a) this magnitude corresponds to the mixture of -0.27(EB-EY) and -0.72(ER-EY) signals. This represents 1.42 times the EG-EY signal.

Let us prove that the output for this case represents 1.42 times the EG-EY signal. Assume that (EG-EY)' is equal to 1/1.42 times the output signal. By multiplying the output by 1/1.42, we get an equation for (EG-EY)' as given in formula 4.1.

$$(EG\text{-}EY)' = (-1/1.42)\ [0.72(ER\text{-}EY) + 0.27(EB\text{-}EY)] \ldots . 4.1$$

To prove that (EG-EY)' is equal to EG-EY, we start with the equation for the luminance EY signal as given by

$$EY = 0.30ER + 0.59EG + 0.11EB$$

We can rewrite this equation as

$$(0.3 + 0.59 + 0.11)EY = 0.30ER + 0.59EG + 0.11EB$$

If we transfer all terms to the left and group them, we get the following equation:

$$0.3(ER\text{-}EY) + 0.59(EG\text{-}EY) + 0.11(EB\text{-}EY) = 0$$

Simplifying the equation, we arrive at the following equations:

$$EG\text{-}EY = -[0.51(ER\text{-}EY) + 0.19(EB\text{-}EY)] \ldots . 4.2$$

or,

$$EG\text{-}EY = -(1/1.42)[0.72(ER\text{-}EY) + 0.27(EB\text{-}EY)] \ldots . 4.3$$

We can see that formula 4.3 is equal to formula 4.1. Thus we have proved that the sum of the ER-EY and EB-EY signals at the output of the demodulator when the subcarrier has a phase angle of 237 degrees is indeed 1.42 times the EG-EY signal.

The colour-subtraction demodulation circuit where three colour-subtraction signals (ER-EY, EB-EY and EG-EY) are taken out directly from the chroma signal is called the three-axis colour-demodulator circuit.

There is another kind of colour-demodulation circuit called the two-axis demodulator circuit. In the two-axis demodulator circuit, only two colour-subtraction signals (ER-EY and EB-EY) are taken out. These two colour-subtraction signals are matrixed to form the EG-EY signal. As given by formula 4.2 the EG-EY signal is composed of 51 per cent ER-EY signal and 19 per cent EB-EY signal.

Another demodulator circuit is the XZ demodulator circuit. As shown in Figure 4-22, when the subcarrier has a phase of 260.5 and 203 degrees, the EX and the EZ signals are taken at the output, respectively. Both EX and EZ signals have components of ER-EY and EB-EY signals.

The EX and EZ signals are not special colour-subtraction signals. They are simply signals having both ER-EY and EB-EY signal components. However, as shown in (a) the red signal is the major component of the EX signal; the blue signal, the major component of the EZ signal.

260.5 degrees and 203 degrees are chosen as the phase of the subcarrier signal because they make it easier to get the ER-EY, EB-EY and EG-EY signals in the succeeding matrix circuit. This procedure in getting the ER-EY, EB-EY and EG-EY signals is called the XZ-axis demodulation system.

Colour-subtraction signal demodulator circuits

Three-axis demodulator circuit. Figure 4-23 shows a three-axis colour-subtraction signal demodulator circuit. The circuit consists of three independent demodulation circuits supplied with their respective subcarrier signals. Each demodulation circuit has identical operations. Figure 4-24(a) shows a single demodulator circuit. Its equivalent circuit is shown in (b).

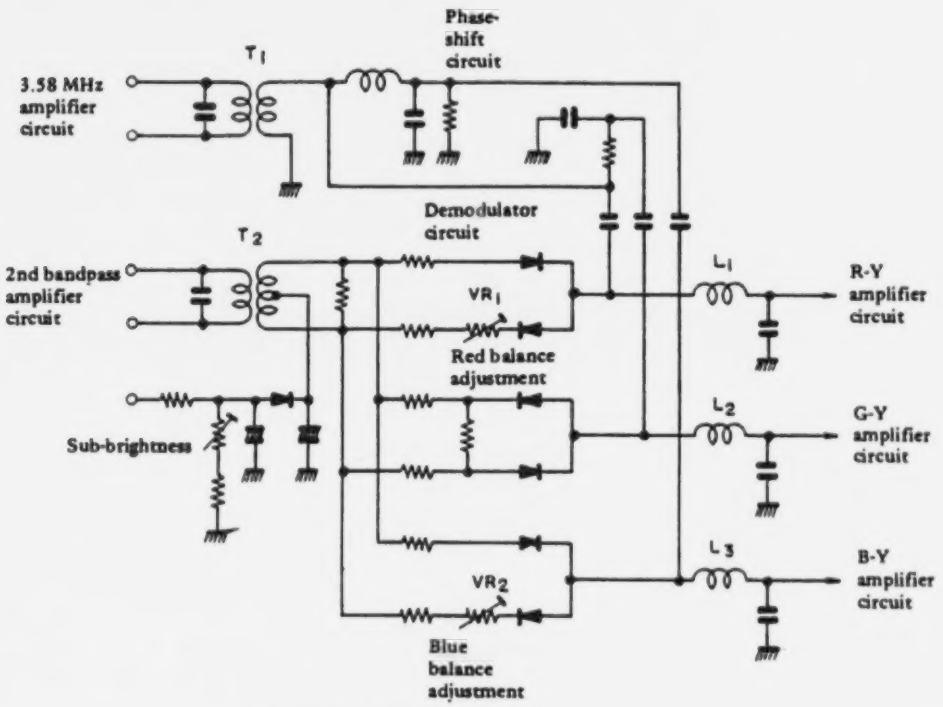


Figure 4-23
Colour-subtraction signal demodulation circuit, three-axis demodulation

When the chroma alone is supplied. As shown in (c) the current flow in D1 and D2, respectively represented by i1 and i2, charges C opposite. Since i1 is equal to i2, the net charge across the capacitor is zero. Therefore the output is zero.

When the subcarrier signal alone is supplied. As shown in (d) the current flow in D1 and D2 charges C opposite. As in (c) the output is zero.

When the chroma and subcarrier signals are supplied together. When the chroma and subcarrier signals are supplied to the circuit, the output voltage varies with the switching time of D1 and D2 and the polarity of the chroma signal.

Figure 4-25 shows six different cases of phase relations between the chroma and the subcarrier signals for each half-cycle of the subcarrier signal.

The amplitude of the subcarrier signal is greater than that of the chroma signal, making the switching of the diode dependent on the polarity of the subcarrier signal.

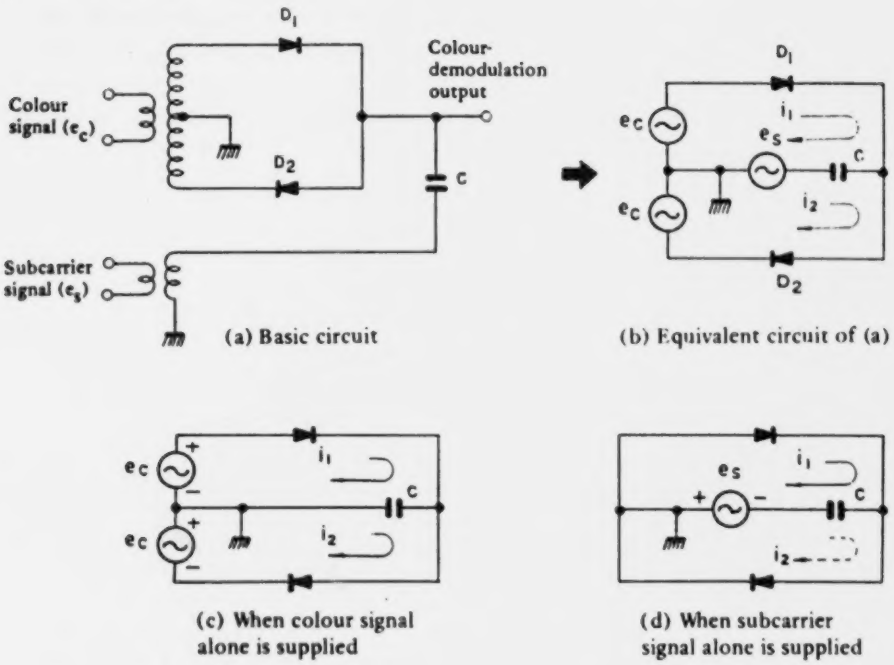


Figure 4-24
The detailed function of a colour-demodulation circuit

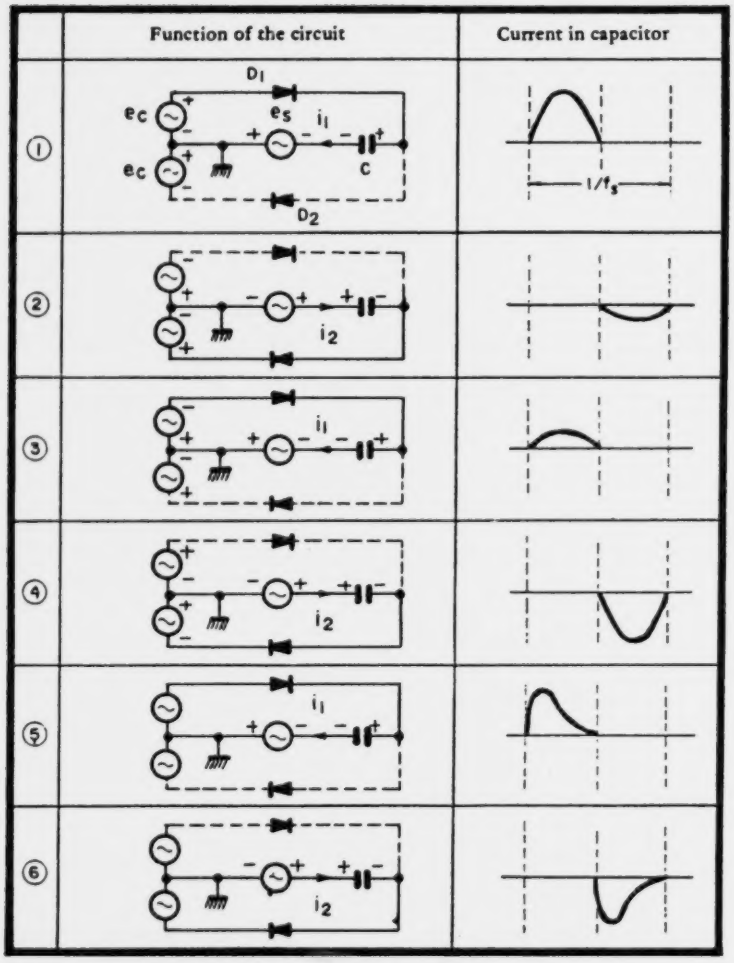
The direction of the current flow depends on the polarity of the subcarrier signal, and the magnitude of the current through the diode (also through the capacitor) is controlled by the chroma signal. The magnitude and polarity of the current flow through the capacitor for each phase relation are shown on the right side of the chart. The demodulator output is taken across the capacitor.

Figures 4-25(1) to (6) show every half-cycle of the subcarrier signal. Since the subcarrier signal is a sine wave, the pairs of cases (1)(2), (3)(4) and (5)(6) form one output cycle. Figure 4-26 shows few cycles in the demodulator output.

When the chroma and subcarrier signals are in phase, a large positive current flows through the capacitor during the positive cycles of the signal. In the negative cycles a small negative current flows through the capacitor. Thus the net output in one cycle of the signals is a positive voltage.

When the signals are 180 degrees apart, the net output voltage is negative, since the magnitude of the negative current exceeds the magnitude of the positive current.

As shown in Figures 4-25 (5) and (6), when the phase difference between the two signals is 90 degrees, the current flow through the capacitor during the positive cycles is equal and opposite to that of the negative cycles. Thus a net negative output signal is produced. This is also the case when the phase difference between the signals is 270 degrees. The phase of the subcarrier signal is controlled by the burst signal but remains constant in magnitude.



Assume the direction of i1 is positive

Figure 4-25
The phase relation of chroma and colour subcarrier signals and its output current

On the other hand, the amplitude and phase of the chroma signal vary with the amount of colour in the image. Therefore the output of the colour-demodulator circuit varies continuously.

The output voltage becomes maximum when the two signals are in phase or 180 degrees apart. The output becomes zero when the phase difference is 90 or 270 degrees. The amplitude of the output signal varies linearly with the magnitude of the chroma signal. Figure 4-22 shows the relationship between the phase difference of the signals and the demodulator output when the amplitude of the chroma signal is kept constant.

As mentioned earlier, the chroma signal is a mixture of two DSB signals 90 degrees apart (ER-EY and EB-EY). Proper colour can be reproduced easily by selecting the phase of the subcarrier signal. This means if a subcarrier signal with a phase exactly the same as the subcarrier signal modu-

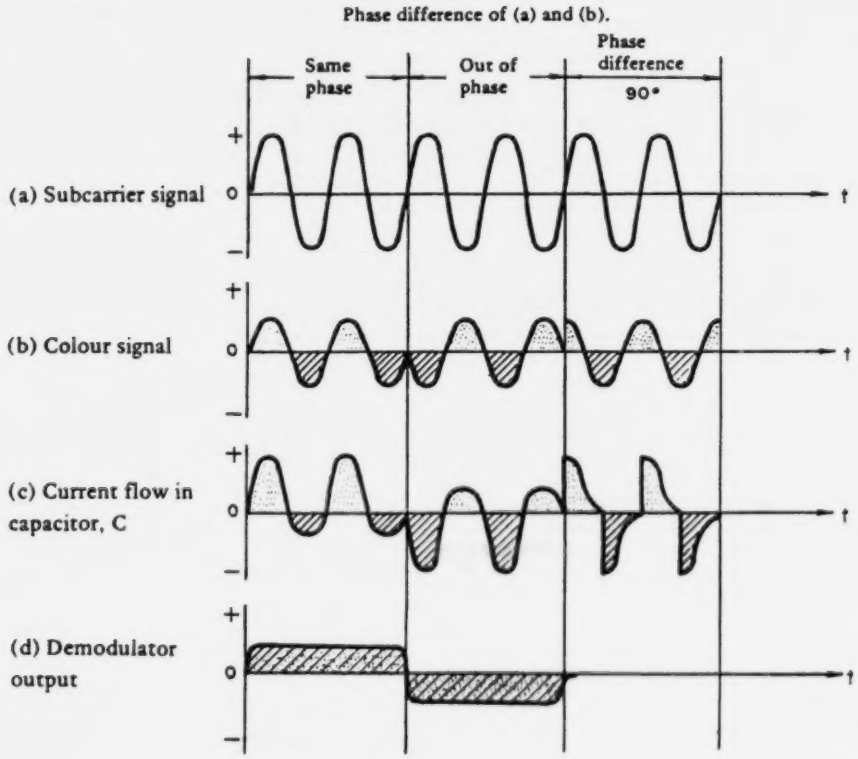


Figure 4-26
Functional wave-forms in a colour-demodulation circuit

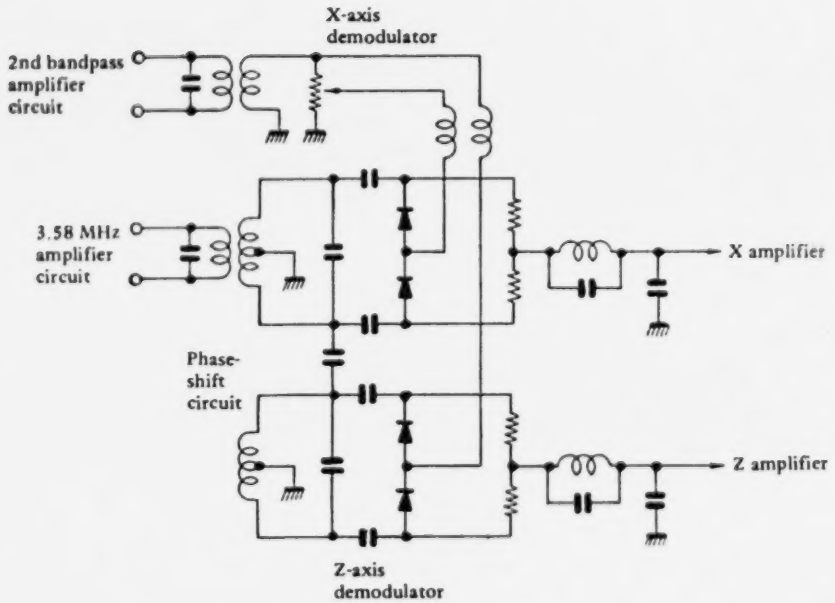


Figure 4-27
An XZ-axis demodulator circuit

lated at the TV station is supplied at the demodulator circuit, the ER-EY or the EB-EY signals can be demodulated.

In Figure 4-23 a phase-shift circuit is used to change the phase of the subcarrier signal needed to demodulate the subtraction signals.

The red and blue adjustment controls (VR1 and VR2) will compensate for the difference in the characteristics of the diodes used as demodulators. If the diodes do not have similar characteristics, the white balance (grey scale) of the raster is affected.

Two-axis demodulator circuit. Two colour-subtraction signals (ER-EY and EB-EY) are detected by the two-axis demodulator circuit. The succeeding matrix circuit develops these two colour-subtraction signals to produce the EG-EY signal. The process is done using formula 4.2.

The two-axis demodulator circuit is commonly used in IC colour receivers. It is not commonly used in transistor receivers, because the circuit becomes complicated using conventional parts.

XZ-axis demodulator circuit

Figure 4-27 shows an XZ-axis demodulator circuit. This circuit works like the two-axis demodulator circuit except when selecting the phase of the subcarrier signal. The phase of the subcarrier signal is set to a value such that the demodulator outputs are the EX and EZ signals as discussed in the section on "Principle of Demodulation."

The subcarrier signal is taken out from the B-Y axis and the phase of the subcarrier signals is selected at 260.5 and 203 degrees for the X and Z axes, respectively.

Colour matrix and output circuit

Structure and function of the circuit

The three electron beams of the colour cathode-ray tube (CRT) must be modulated by the colour signals to reproduce a colour image on the screen. There are two systems used in modulating the electron beams—the primary-colour drive and the colour-subtraction drive.

In the primary-colour drive system, the three colour signals (ER, EG and EB) are modulated with the luminance (EY) signal before they are supplied to the CRT. The modulated signals are usually supplied to the respective cathodes of the colour CRT. This type is commonly used in solid-state colour TV sets.

In the colour-subtraction system, the colour-subtraction signals (ER-EY, EG-EY and EB-EY) and luminance signal (EY) are independently supplied to the different electrodes (first grid and cathode, respectively) of the colour CRT. (See Figure 4-1.)

To reproduce colour images on the screen, it is necessary to supply to the colour CRT either the three primary-colour beams modulated with the luminance signal or the colour-subtraction and luminance signals together. These signals must have enough amplitude to drive the colour CRT. The colour output circuit amplifies the demodulated colour signals to a level enough to drive a colour CRT.

The output of the colour demodulator circuit is either the colour-subtraction signals or the XZ-axis signals, depending on the type of the demodulator circuit used. These signals must be converted into either three primary-colour signals or colour-subtraction signals, depending on the drive system used in driving the CRT.

A matrix circuit converts the output of the colour-demodulator circuits into the signals required by the colour CRT drive circuit used. The function of the matrix circuit varies with the type of demodulator circuit and the drive system. The functions of the matrix circuits are summarised below.

Two-axis demodulation circuit. The matrix circuit develops the ER-EY and the EB-EY signals to form the EG-EY signal.

XZ-axis demodulation circuit. The matrix circuit forms the ER-EY, EG-EY and EB-EY signals from the EX and EZ signals.

The primary-colour drive system. The matrix circuit adds the luminance signal (EY) to the three colour-subtraction signals (ER-EY, EG-EY, EB-EY) and produces three primary-colour (ER, EG and EB) signals.

Matrix circuit of the primary-colour drive and its output circuit

Figure 4-28 shows a primary-colour drive circuit. The three colour-subtraction signals and the luminance signal are supplied to the colour output circuit. The colour output transistors Q1, Q2 and Q3 are used in a common-base configuration with respect to the luminance signal and in common-emitter configuration with respect to the colour-subtraction signals.

The transistors develop and amplify the colour-subtraction and luminance signals to produce the three primary-colour signals to drive the colour CRT.

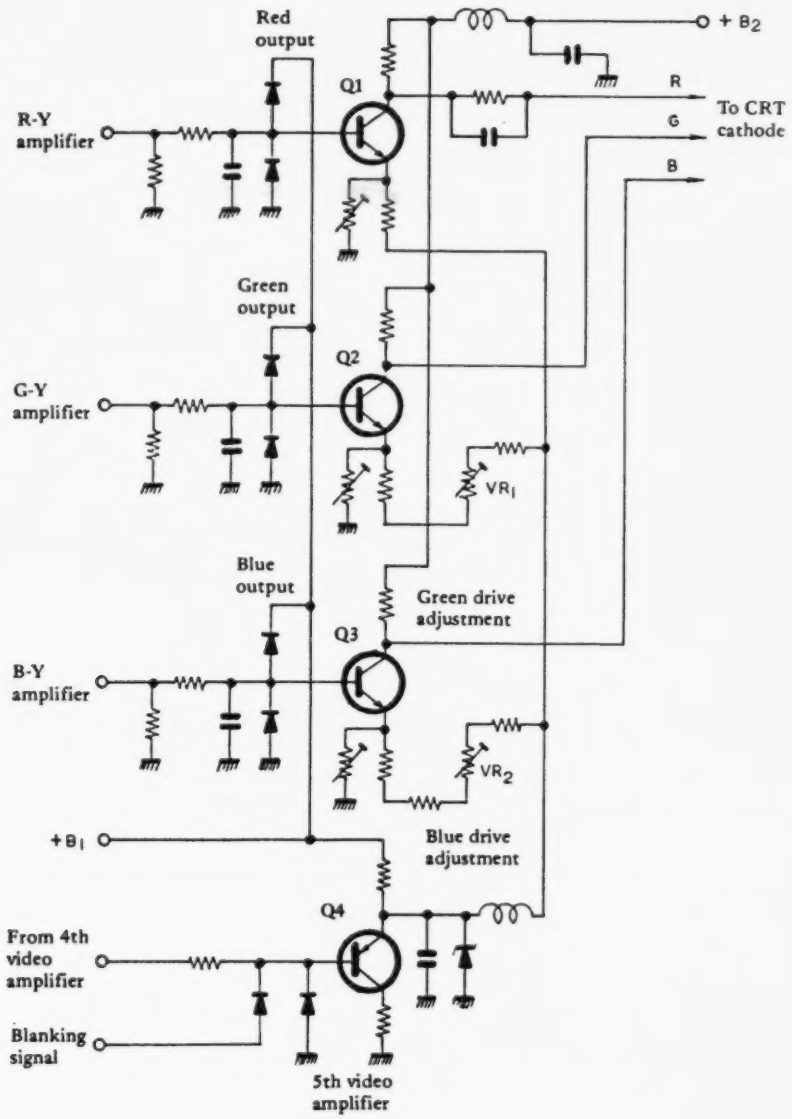


Figure 4-28
A primary-colour drive circuit

The drive-adjustment resistors VR1 and VR2 set the level of the EG-EY, EB-EY and EY signals for the proper beam ratio of the three primary colours.

Matrix circuit of the colour-subtraction drive and its output circuit

Figure 4-29 shows a colour-subtraction drive output circuit. The EX and EZ signals from the demodulator circuit are amplified by the X and Z amplifier circuits, respectively. The output circuit also functions as a matrix circuit. In principle, the base of the G-Y amplifier transistor is grounded on the signals, as shown in Figure 4-30.

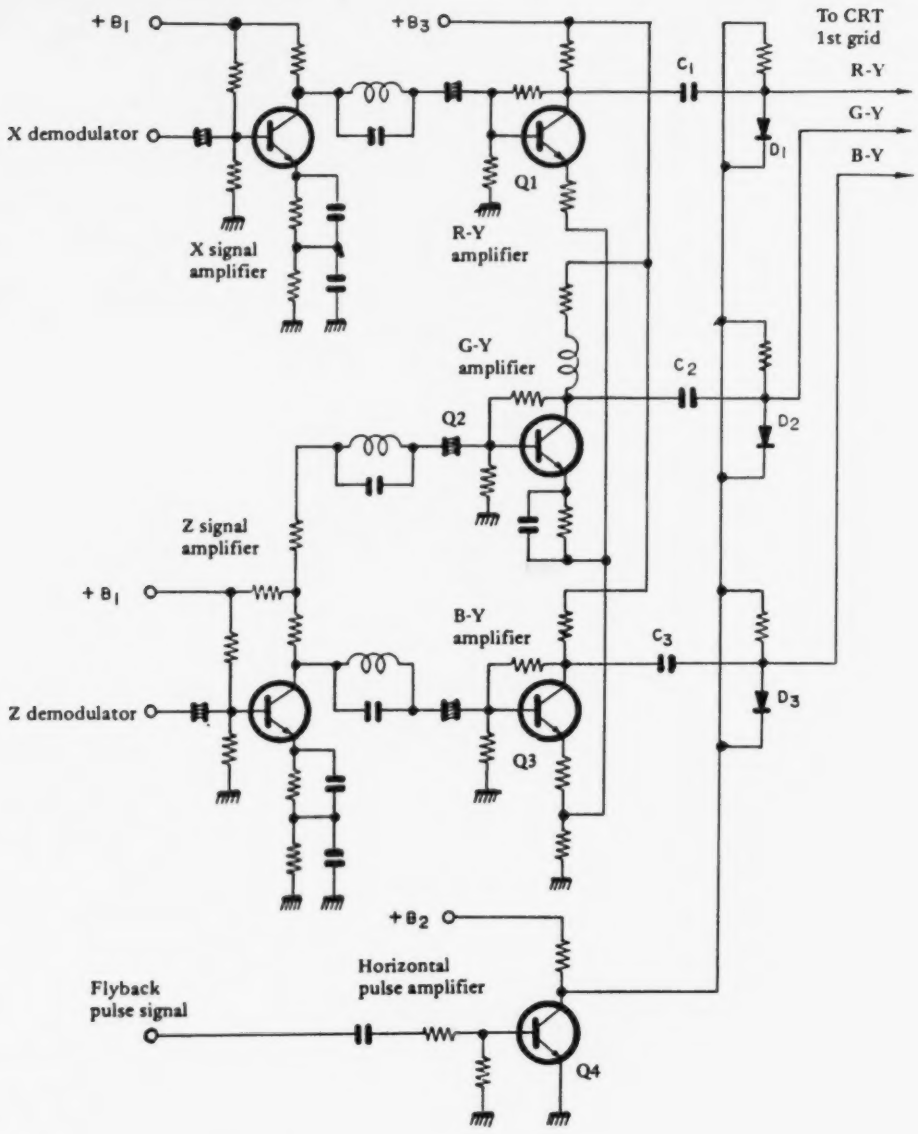


Figure 4-29
A colour-subtraction drive output circuit

In Figure 4-30, when the EX and EZ are supplied to the output transistors Q1 and Q3, a voltage is generated across the common-emitter resistor RE. This voltage is denoted by EE (Figure 4-30). Thus the base-emitter voltages (Vbe) across Q1 and Q3 are EX-EE and EZ-EE, respectively. The voltage across RE is supplied to the emitter of Q2. Therefore if the EX and EZ signals such as the EX-EE = -(ER-EY) and the EZ-EE = -(EB-EY) signals, and EE = (EG-EY) are supplied from the demodulator circuit, the three colour-subtraction signals ER-EY, EB-EY and EG-EY are obtained at the collector circuit of Q1, Q2 and Q3, respectively.

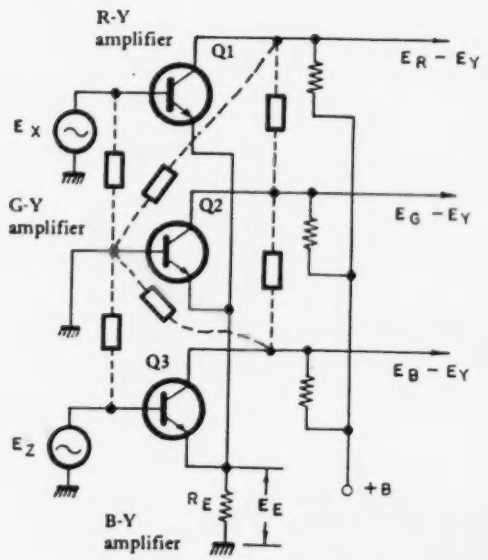


Figure 4-30
Matrix circuit made out of common-emitter circuits

DC restoration circuit

If the DC component of the colour-subtraction signals produced by the colour-demodulation circuit is not completely coupled to the colour CRT, the hue or colour of the reproduced image deviates from the original. For example, if the background colour changes, the colour of the object also changes.

In Figure 4-29 the DC component of the collector signal of the colour output transistors is not coupled to the first grid of the colour CRT, because the collector outputs are AC-coupled to the CRT by capacitors C1 to C3. Thus colour is not properly reproduced.

Figure 4-31(a) shows part of the colour-subtraction signal output circuit, shown in Figure 4-29. The colour-subtraction signal demodulated by the demodulator circuit is not symmetrical to the level shown in (b). This is the reference level.

If this kind of signal is capacitively coupled to the circuit shown in (c), the current flow at the positive cycle of the colour-subtraction signal charges C. When this happens, the reference level of the colour-subtraction signal is shifted by EC (voltage across the capacitor), as shown in (d).

The magnitude of EC is proportional to the amplitude of the colour-subtraction signal. This voltage varies the bias of the CRT. Even if the level of the colour-subtraction signal is constant, the bias voltage of the CRT is still shifted. This makes proper colour reproduction impossible.

To get proper colour reproduction, a DC restoration circuit is used to restore the DC component of the signal. For this purpose, the voltage stored in capacitor C is discharged during the horizontal retrace period.

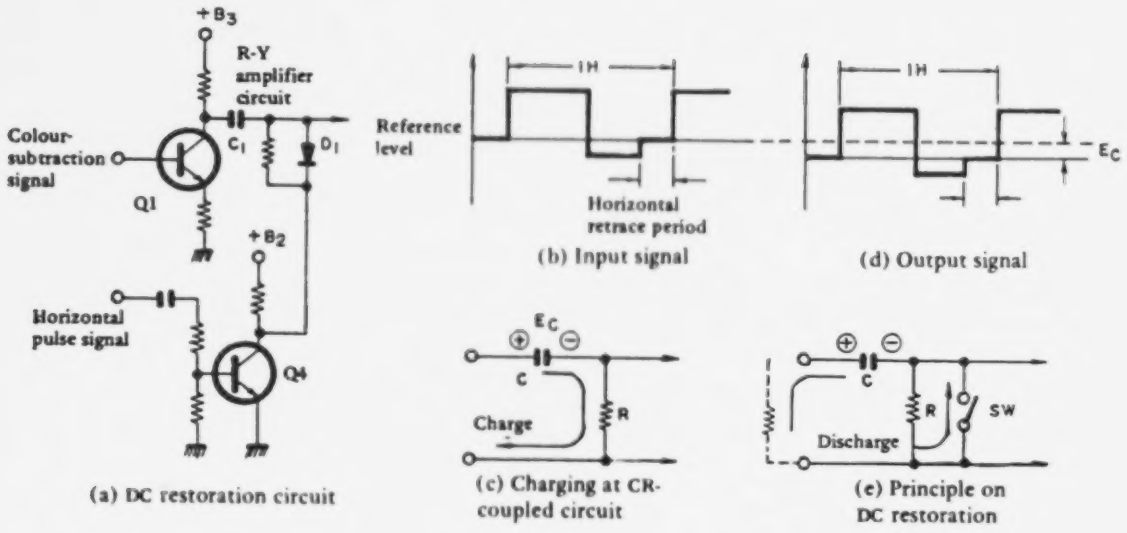


Figure 4-31
DC generator circuit and its principle

A switch shown in Figure (e) is closed during the horizontal retrace period and discharges C. When the capacitor is discharged, the level of the colour-subtraction signal returns to its original level. Thus even when the colour-subtraction signals are capacitively coupled to the CRT, its level is maintained at reference level. Thus proper colour is reproduced.

In the actual circuit shown in (a) the switch SW is replaced by D1. Q4 is keyed on by the horizontal sync pulses during the horizontal retrace periods. When Q4 conducts, the collector voltage decreases and D1 starts to conduct. When D1 conducts, C1 discharges through it. Thus the colour-subtraction signal is coupled to the CRT at the proper reference level.

Chroma-signal processing circuit by inductive coupling (IC)

The block diagram

The inductive coupling chroma-signal demodulation circuit processes the chroma signal into the colour-subtraction signals. In modern colour TV sets this function is performed by a single IC. Some receivers, however, use more than one IC.

It is difficult to include capacitive and inductive components within an IC chip. To reduce discrete components, the design of the IC chroma-signal processing circuit is very different from the conventional solid-state circuit.

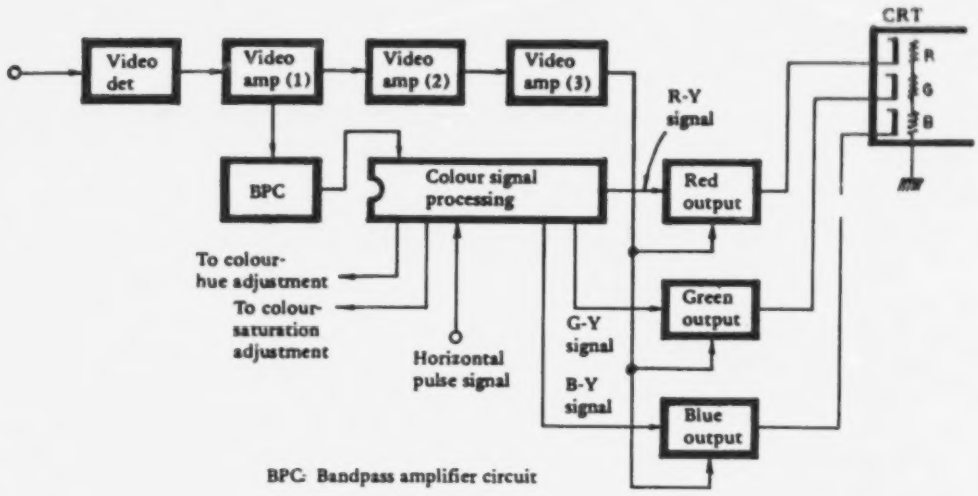


Figure 4-32
Functional block diagram of IC colour signal processing circuit

Figure 4-33 shows a chroma-signal processing circuit using a single IC. The principle involved in circuits using more than one IC is similar. Instead of an IC performing the entire operation, the function is divided among two or three ICs.

In Figure 4-32 the composite video signal which includes the chroma signal is taken out from the video pre-amplifier circuit and then fed to the bandpass amplifier circuit. Since the circuit has a narrower bandwidth and tuned to the frequency of the chroma signal, the output consists only of the amplified chroma signal. The signal is then fed to the IC. The IC processes the chroma signal into the colour-subtraction signals (ER-EY, EG-EY and EB-EY) and then supplies them to the output transistors.

In the block diagram shown in Figure 4-32, transistors are used for the colour output circuit. This is because the CRT drive circuit used in the block diagram of Figure 4-32 is a primary-colour drive circuit, which requires around 100 Vp-p to drive the colour CRT. An IC is not capable of handling such a high-level signal.

Transistors are also used at the output to protect the IC from the internal static discharge of the colour CRT. The structure of the oscillator and detector circuit within the IC chip varies slightly with the circuits of other ICs. However, their functional block diagrams are similar.

Function and internal block diagram of an IC used for chroma-signal reproduction

Figure 4-33 shows an internal block diagram of an IC used in the chroma-signal reproduction circuit. This IC performs the entire chroma-signal processing.

The chroma signal is fed to the input pin 15. From pin 15, the signal is fed to the gain-control circuit through the first and second bandpass circuits. The horizontal flyback pulses fed at pin 13 are used by the gate circuit for clipping the burst signal. The clipped burst signal is then fed to the ACC circuit, which detects the magnitude of the burst signal to produce a DC-control voltage for the gain control of the first bandpass amplifier circuit.

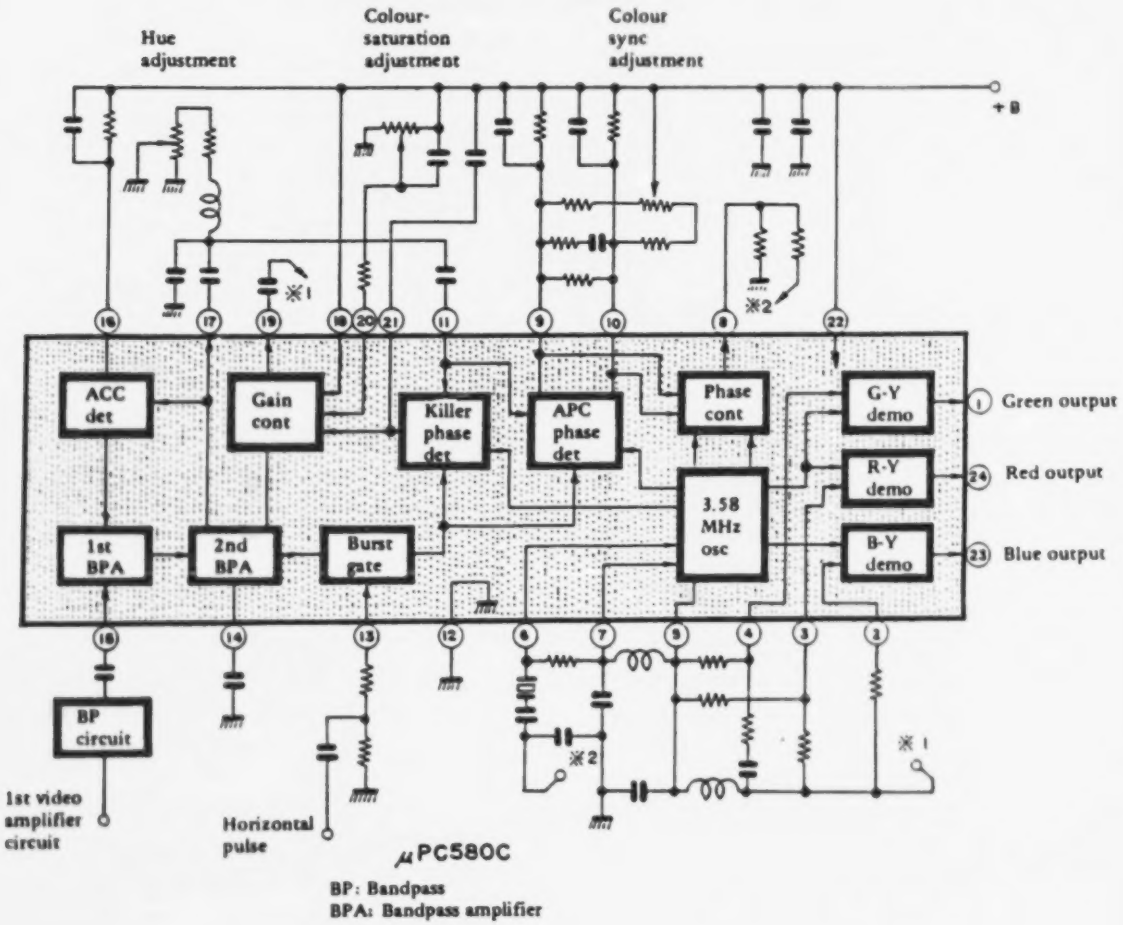


Figure 4-33
An IC colour signal processing circuit

The burst signal is also fed to the hue-control circuit through pin 17. The burst signal is fed back to the IC through pin 11 for the colour-killer and APC functions. The chroma signal with the burst signal separated by the gate circuit is fed to the colour-saturation circuit. This circuit controls the magnitude of the colour and is outside the IC.

The gain-control circuit regulates the chroma signal through the colour-killer and colour-saturation adjustment. The regulated signal is taken out from pin 19 and then fed to the colour-demodulator circuits (R-Y, G-Y and B-Y) through pins 2, 3 and 4.

The subcarrier signal generated by the 3.58 MHz oscillator circuit is supplied to the colour-demodulator, colour-killer, APC and phase-control circuits.

The APC circuit is composed of a phase-detector circuit. It compares the phase of burst signal from pin 11 with the phase of the subcarrier signal. When a phase difference is detected, the phase detector produces a control voltage to lock in the phase of the subcarrier to the phase of the burst signal.

The phase-detector circuit is also used by the colour-killer circuit. The absence of the burst signal is detected by the phase-detector circuit during monochrome transmission, and the colour-killer circuit is disabled by the gain-control circuit. (See Figure 4-33.)

Dynamic function of the chroma IC

Inductive couplings are purely made of semiconductor materials. The amplifiers within an IC are coupled directly.

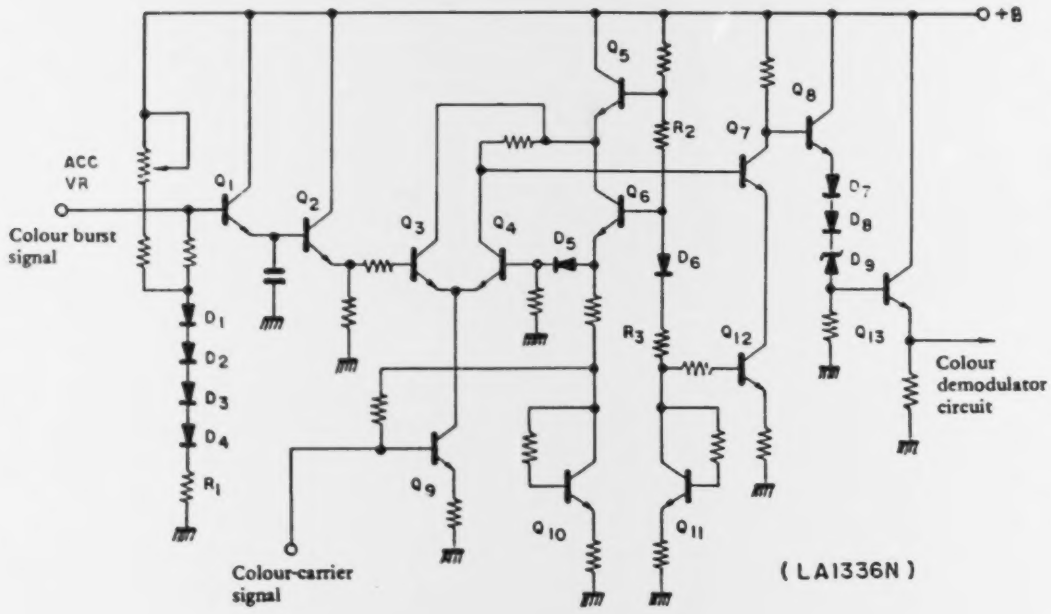


Figure 4-34
Equivalent circuit of an IC used for bandpass amplifier circuit

The operation of the IC is much affected by changes in the surrounding temperature and the supply voltage. To prevent changes in the IC's characteristics during operation, the power-supply circuit should be precise and the IC should operate in normal temperatures. However, as described in the section "Subcarrier Signal Generator Circuit," the supply voltage of the IC is varied to change the level and frequency of the signal within the IC.

Figure 4-34 shows the internal circuit of an IC bandpass amplifier circuit.

The chroma signal is amplified by transistors Q9, Q4, Q7, Q8 and Q13. Q1, Q2 and Q3 are used for the ACC function. The burst signal, which is proportional to the magnitude of the chroma signal, is fed to Q1 and detected.

A DC voltage proportional to the magnitude of the burst signal appears across the emitter capacitor of Q1. This DC voltage is amplified by Q2 and supplied to Q3. The collector current of Q3 changes with the magnitude of the burst signal.

Q9 functions as a current regulator. The current flowing through Q9 is the sum of the current flow through Q3 and Q4. The change in collector current of Q3 affects that of Q4.

When the level of burst signal increases, the collector current of Q3 increases, while the collector current of Q4 decreases. Therefore the gain of Q4 is decreased and ACC action is performed. The ACC action is externally controlled by variable resistor VR, which varies the base voltage of Q1.

The following paragraphs further explain the circuits used within the bandpass amplifier IC shown in Figure 4-34.

Differential amplifier circuit. This circuit stabilises the operation of the IC with respect to changes in supply voltage and temperature.

In Figure 4-34 the transistors Q1, Q2, Q3, Q4 and Q6 and D5 form differential amplifier circuits. Q1, Q2 and Q3 are symmetrical to Q4, D5 and Q6, respectively. They maintain the balance of the differential amplifier circuit.

Voltage regulator circuit. This circuit is formed by Q5, D6 and Q11. The regulator circuit prevents the shifting of the operating point of Q7.

Q11 merely functions as a diode and maintains the base voltage of Q6 together with D6 despite changes in the supply voltage and temperature. When Q6 has a stable base voltage, the base voltages of Q4 and Q7 and the emitter voltage of Q6 are also stabilised.

DC-level shift circuit. Diodes D7 to D9 form a DC-level shift circuit. This circuit makes the emitter voltage of Q8 equal to the base voltage of Q13. Zener diode D9 actually sets the voltage of the DC shift level.

D7 and D8 compensate for the changes in the characteristic of D9 due to changes in temperature. The voltage across D9 increases when its temperature increases. However, D7 and D8 are in series with D9. When the temperature increases, the voltage drop across D7 and D8 decreases and compensates for the voltage increase across D9. Hence the overall DC shift level is not altered.

Temperature compensation circuit. The voltage (Vbe) across the base-emitter junction of a transistor decreases with the increase in temperature. When the voltage supply to the base is kept constant, an increase in temperature will increase the base current and increase the collector current. An increase in the collector current changes the dynamic function of the transistor.

To prevent changes in the dynamic function, a compensating circuit is used to keep the base current constant by decreasing the base voltage when the temperature increases.

In Figure 4-34, D1 to D4 compensate for the changes in the base-emitter voltages of Q1 to Q3.

When the temperature increases and Vbe of the transistors decreases, the voltage between the anode and cathode of the diodes also decreases. This decrease in the voltage keeps the base current of the transistor constant. Thus the initial decrease in the base-emitter voltage is compensated. D6, Q11 and Q12 perform the same function to compensate for the changes in the voltage of Q4, D5 and Q6.

The voltage changes in the base-emitter junction of Q9 and Q12 are compensated by Q10 and Q11, respectively.

The structure of the circuit within the IC chip looks very complicated. The complication, however, is due to the compensation circuit used for stabilising the circuit's operation despite changes in the temperature and supply voltage.

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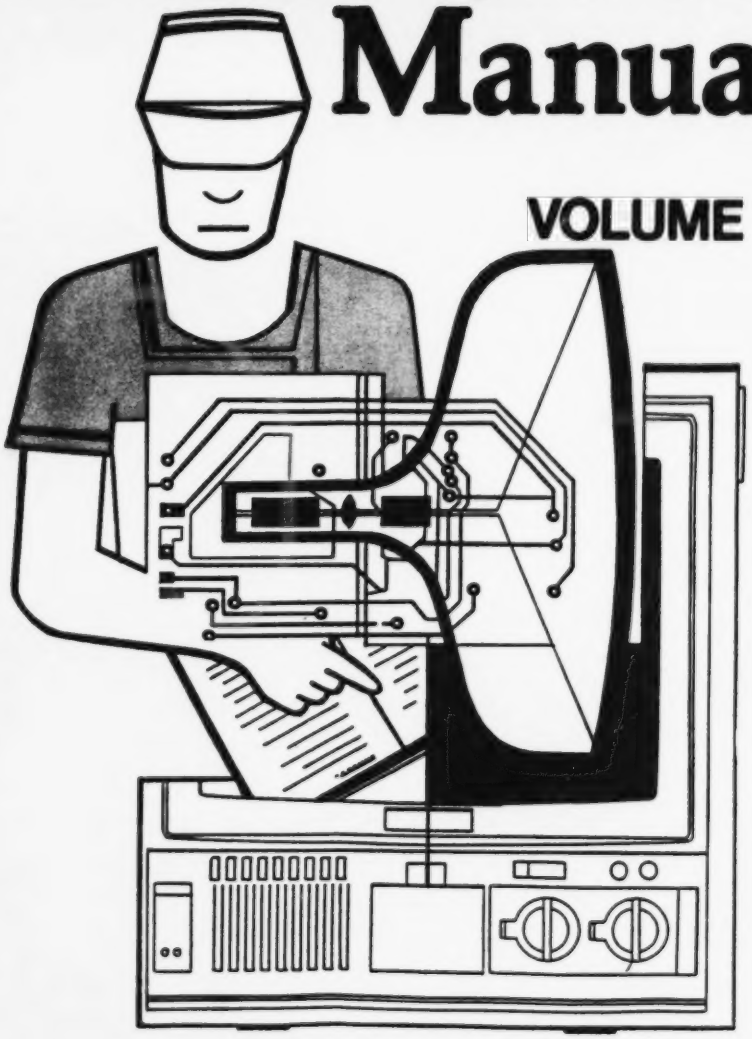

BY MASAAKI MUKAI AND RYOZO KOBAYASHI

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TV Trouble-shooting Manual

VOLUME 10

BY MASAAKI MUKAI AND RYOZO KOBAYASHI

Part 4: Chroma-signal reproduction circuit (Instructor's manual)

ASIAN AND PACIFIC SKILL DEVELOPMENT PROGRAMME
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Part 4: Chroma-signal reproduction circuit

Block diagram of a chroma-signal reproduction circuit

Figure 4-1 shows block diagrams of three chroma-signal reproduction circuits.

There are two types of video-detector circuits used in distinguishing the chroma signal from the composite video signal. One uses the same diode for detecting the luminance and chroma signals, as shown in Figures 4-1(a) and (b). The other [Figure 4-1(c)] uses two diodes, one for detecting the luminance signal and the other for the chroma signal. The chroma signal is processed (or demodulated) further by either the colour-subtraction or the XZ demodulation circuit.

In the colour-subtraction demodulation circuit, either two or three colour-subtraction signals (ER-EY and EB-EY or ER-EY, EG-EY and EB-EY) are directly taken out from the output of the demodulation circuit, as shown in (a) and (c). In the XZ demodulation circuit, the EX and EZ signals are taken out. The EZ and EX signals are then matrixed by the succeeding stage to produce the R-Y, G-Y and B-Y signals, as shown in (b).

With the introduction of colour-demodulator circuits using an inductive coupling (IC), the colour-subtraction demodulator circuit, with three primary-colour drive circuits, as shown in (a) and (c), is commonly used in modern colour receivers.

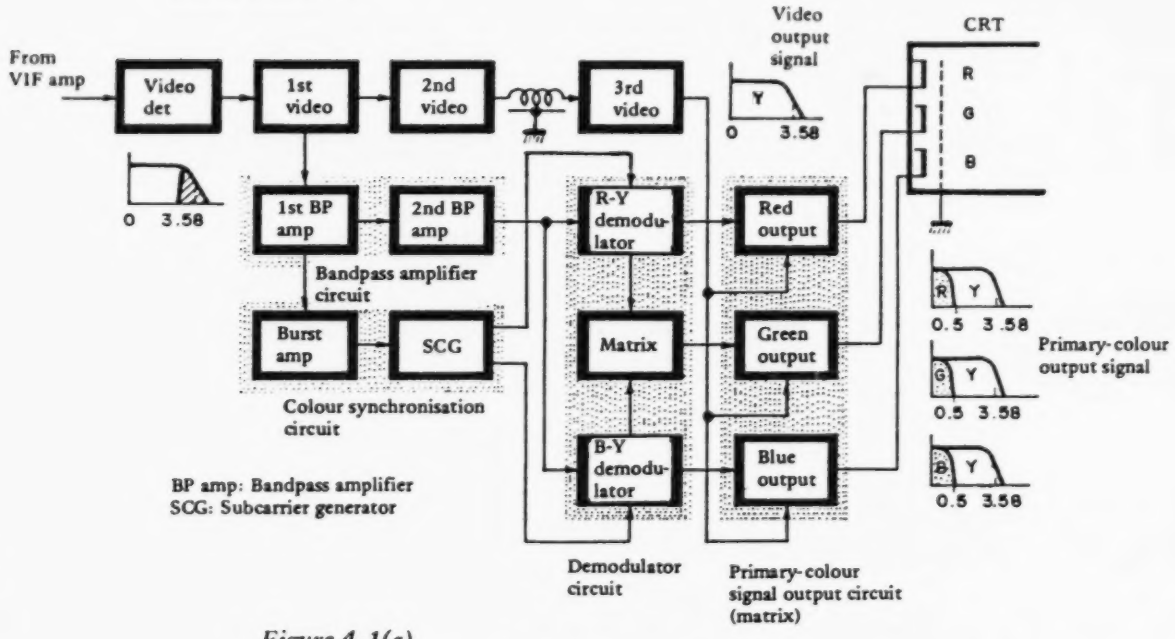


Figure 4-1(a)
Chroma-signal reproduction circuit
(Chroma and luminance signals are detected together, colour-subtraction demodulation and primary-colour circuit.)

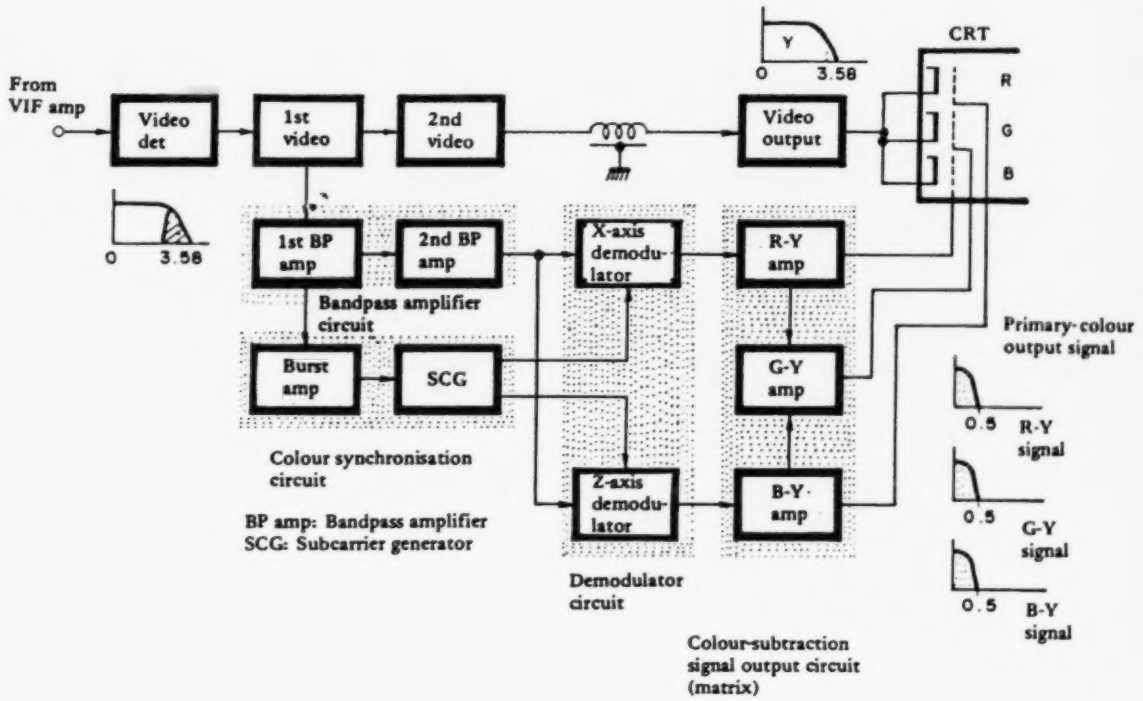


Figure 4-1(b)

Chroma-signal reproduction circuit

(Chroma and luminance signals are detected together, XZ-axis demodulation and colour-subtraction drive circuit.)

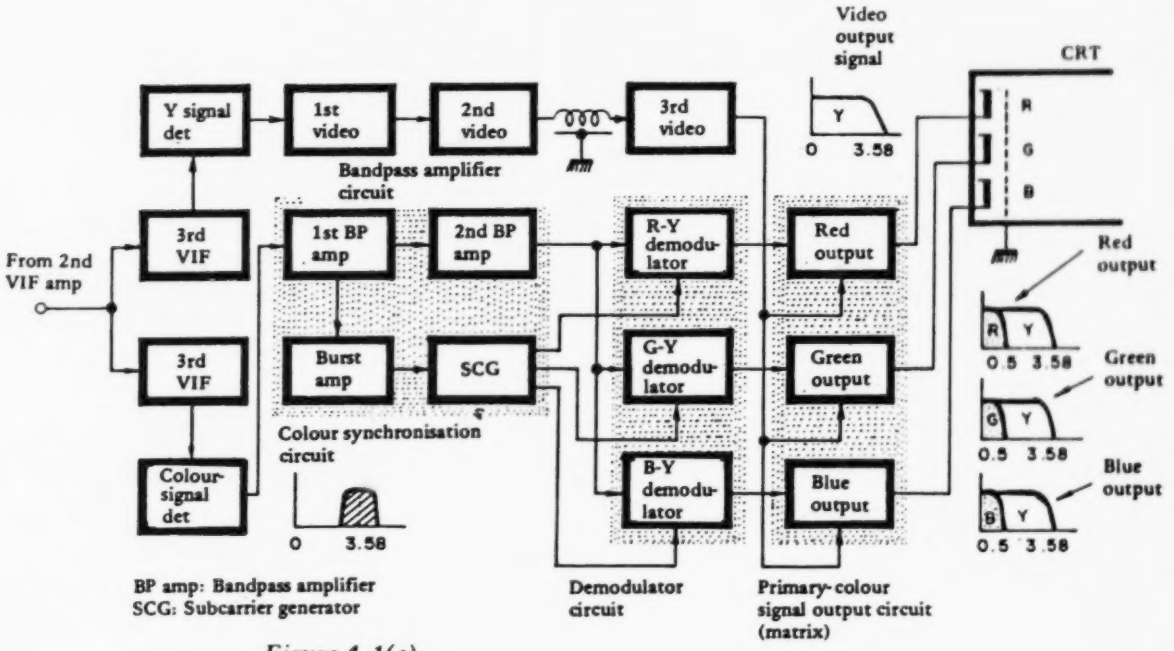


Figure 4-1(c)

Chroma-signal reproduction circuit

(Chroma and luminance signals are independently detected, colour-subtraction demodulation and primary-colour drive circuit.)

The bandpass amplifier circuit

Block diagram of a bandpass amplifier circuit and its functions

Figure 4-2 shows a functional block diagram of the bandpass amplifier circuit. This circuit amplifies the chroma signal and then supplies it to the chroma-signal demodulation circuit. The bandpass amplifier circuit is tuned to 3.58 +/- 0.5 MHz. The following paragraphs discuss the detailed functions of the bandpass amplifier circuit.

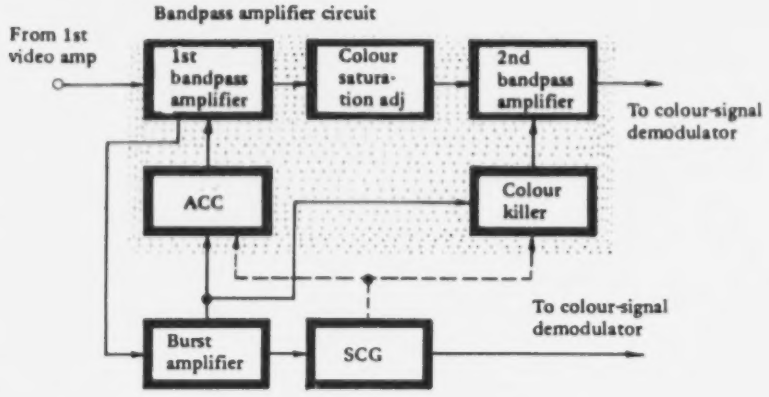


Figure 4-2
Functional block diagram of a bandpass amplifier circuit

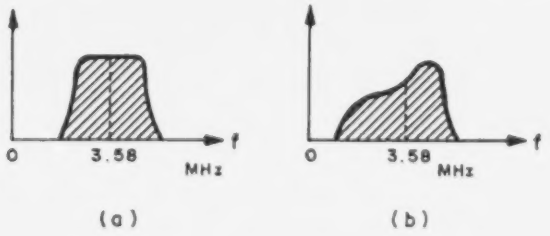


Figure 4-3
Chroma-signal frequency spectrum

It levels the amplitude of the chroma signal within the bandwidth. The chroma signal within the 0.5 MHz bandwidth must be symmetrical at 3.58 MHz, as shown in Figure 4-3(a). If the signal is not symmetrical as shown in (b), proper colour reproduction cannot be obtained, because of the uneven frequency response of the chroma signal.

However, the overall response of the chroma signal is not symmetrical, because it is located at the shoulder of the frequency spectrum of the composite video signal and is affected by the sound trap circuits. As seen in the upper figure in 4-4(a) and (b) the higher components of the chroma signal are attenuated.

The tuning circuit of the first bandpass amplifier circuit compensates the attenuation of the high-frequency components of the chroma signal to make

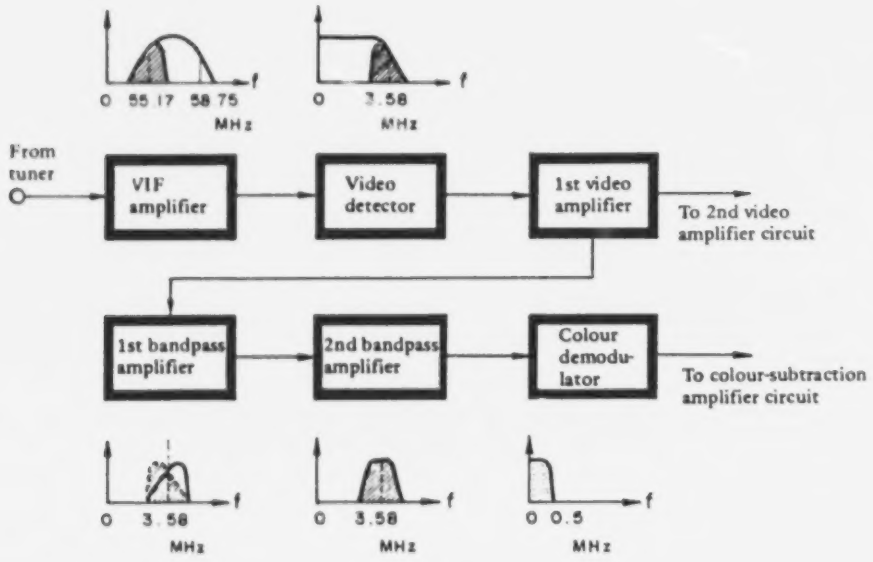


Figure 4-4(a)
Bandpass response
(Chroma and luminance signals are detected together.)

the level or the strength of the sidebands of the chroma signal equal. Figure 4-4 gives the signal flow in the processing of the chroma signal; Figure 4-4(a), the signal flow when the chroma and the luminance signals are detected together; (b), the signal flow when the chroma and the luminance signals are detected independently.

It controls colour saturation. The viewer should be able to adjust the colour-saturation level according to his taste. The colour-saturation level can be varied by adjusting the gain of the bandpass amplifier circuit.

It has an automatic colour-control (ACC) circuit. An automatic level-control circuit called the ACC is used within the bandpass amplifier circuit. It maintains a chroma signal with a constant level despite variations in the TV signal strength or a mismatch in the antenna to maintain a constant colour-saturation level.

This circuit uses the burst signals as a parameter. Variations in the TV signal strength are detected by changes in the level of the burst signals, as shown in Figure 4-2. The ACC circuit either increases or decreases the gain of the bandpass amplifier circuit, depending on whether the strength of the burst signal decreases or increases.

It has a colour-killer circuit. When a black-and-white signal is received, the colour-reproduction circuits should be disabled. Otherwise, the screen will be filled with colour noise or snow. The colour-killer circuit automatically disables the colour-reproduction circuits when a monochrome signal is received.

It prevents the burst signals from penetrating the colour-demodulation circuit. The phase of the burst signals is used as the reference in determining the proper phase of the regenerated colour subcarrier signals for proper colour

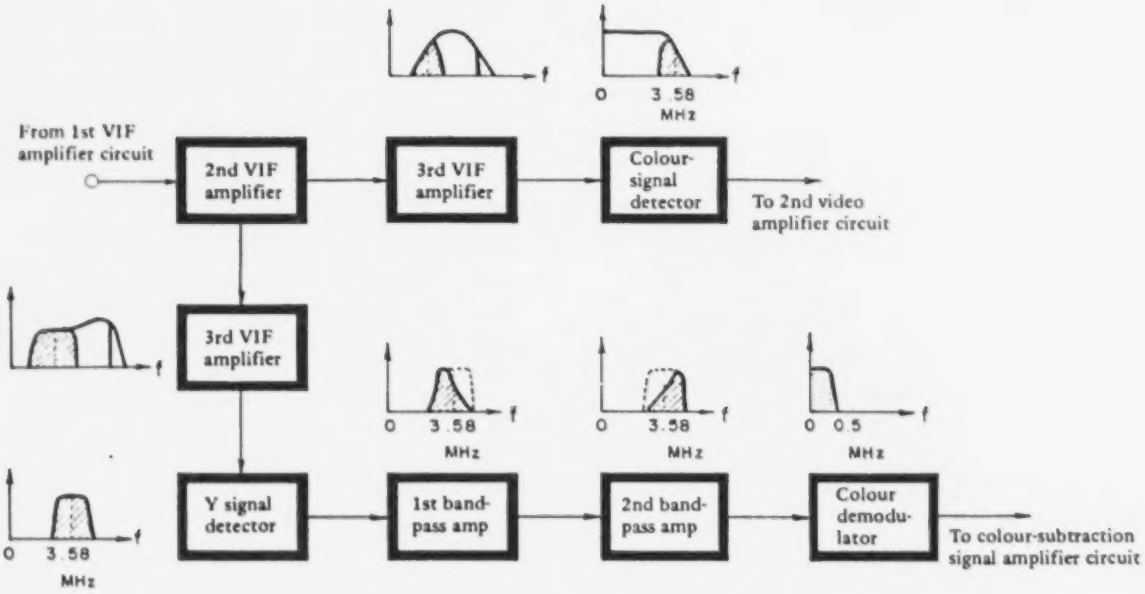


Figure 4-4(b)
Bandpass response
(Chroma and luminance signals are independently detected.)

reproduction. The colour burst signals are transmitted during the horizontal retrace periods to prevent them from interfering with the image on the screen. However, if the DC restoration of the colour-subtraction signal is done during the horizontal retrace period, the colour burst signals will affect the reference level of the DC restoration. To prevent this, the bandpass amplifier circuit is disabled during the horizontal retrace period.

First bandpass amplifier and ACC circuit

The burst signals are detected by the detector circuit in the ACC circuit. The ACC circuit produces a DC-control voltage proportional to the strength of the burst signal. The control voltage is used to control the gain of the first bandpass amplifier circuit.

ACC detector. There are three kinds of ACC detector circuits. Figure 4-5 shows examples of these circuits.

Figure 4-5(a) is an example of a diode detector circuit. The colour burst signals are amplified by the burst signal amplifier transistor Q3. The burst signals are coupled to the ACC detector diode D1 by C1. D1 conducts during the positive half-cycles of the burst signals. The voltage across C1, whose polarity is shown in the figure, is called the ACC voltage. This voltage is supplied to the base of the ACC amplifier transistor Q2.

Figure 4-5(b) shows an ACC transistor-detector circuit. The burst signals are detected by the ACC detector transistor Q3. The burst signals are supplied to the base of Q3 and Q3 conducts during the negative half-cycles. The collector current of Q3 charges C1 and the voltage across it is called the ACC voltage.

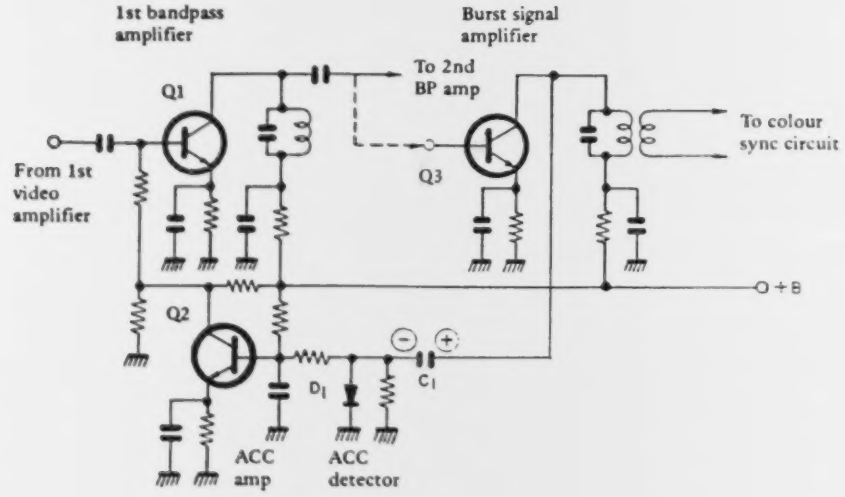


Figure 4-5(a)
Diode ACC detector circuit

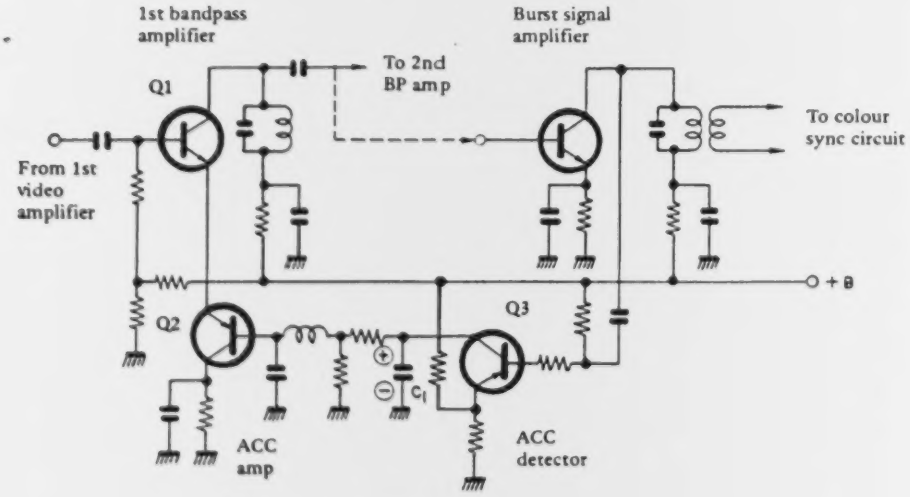


Figure 4-5(b)
Transistor ACC detector circuit

Figure 4-5(c) shows an ACC phase-detector circuit. The colour burst and the colour subcarrier signals are supplied to the circuit. The colour sync circuit synchronises the colour subcarrier frequency with the colour burst signal frequency. The output voltage of the phase-detector circuit (taken at node [P]) is zero if the phase difference between the two signals is 90 degrees.

The output becomes either positive maximum or negative maximum when the two signals are in phase (0 degrees apart) or 180 degrees apart, respectively. However, the two signals supplied to the circuit are designed to have the same phase. Thus the output voltage is positive and its magnitude is proportional to the amplitude of the colour burst signals.

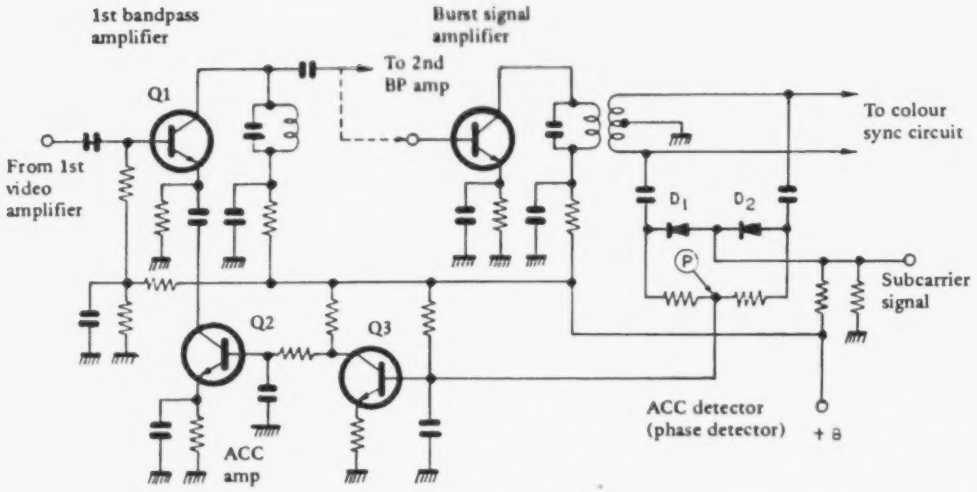


Figure 4-5(c)
ACC detector circuit by phase detector

Besides detecting ACC, the circuit can determine the presence of the burst signals. Thus it is also used for the colour-killer circuit.

Gain control of the first bandpass amplifier circuit. Three circuits can be used to control the gain of the bandpass amplifier circuit. All of them control the gain of the bandpass amplifier circuit if the amplitude of the colour burst signal changes.

In Figure 4-6(a) the gain of the first bandpass amplifier transistor (Q1) is controlled by varying its base voltage. The base voltage is varied by the ACC amplifier transistor Q2.

In (b) the gain of the bandpass amplifier circuit is controlled by varying the amount of the emitter feedback of the bandpass amplifier transistor Q1. The

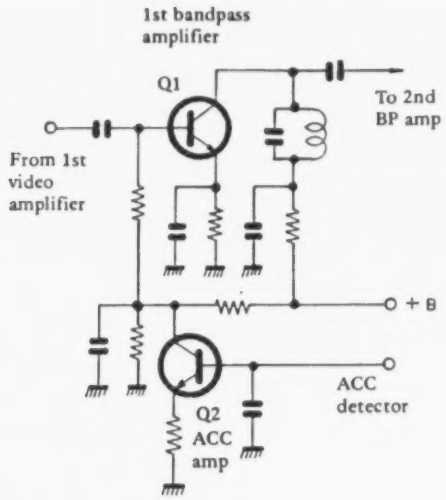


Figure 4-6(a)
Gain control by collector current

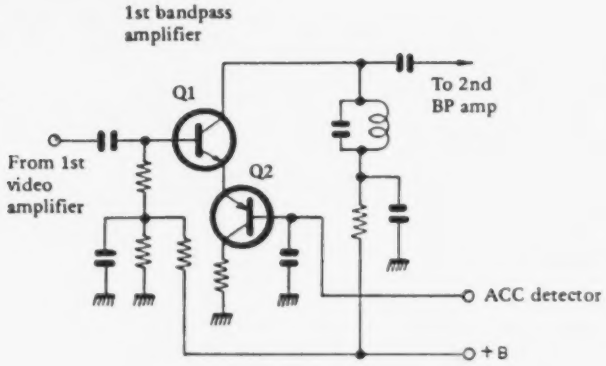


Figure 4-6(b)
Gain control by current feedback

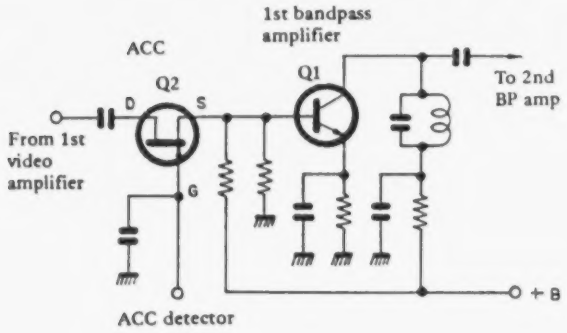


Figure 4-6(c)
Input signal control by a FET

feedback to Q1 is varied by changing the internal resistance of Q2, which is connected to the emitter circuit of Q1. The internal resistance of Q2 can be controlled by the ACC voltage supplied to its base.

In (c) the amplitude of the output of the bandpass amplifier circuit is controlled by a field-effect transistor (FET). The FET is connected in series to the base circuit of the bandpass amplifier circuit. The internal resistance of the FET is controlled by the ACC voltage. In turn, changes in the internal resistance of the FET are reflected as changes in the amplitude of the output of the first bandpass amplifier circuit.

Second bandpass amplifier and colour-killer circuit

The bandpass amplifier circuit must be disabled during black-and-white reception and enabled during colour reception. Colour reception is detected by checking the presence of the colour burst signals. The colour-killer circuit disables the the colour-reproduction circuits during monochrome reception.

Figure 4-7 shows a colour-killer circuit. In (a) a diode is used as the burst signal detector. A reverse bias voltage is supplied to the base-emitter junction of the second bandpass amplifier transistor Q1. Thus Q1 is normally cut off. If the burst signals are present, D1 conducts during the positive half-cycles and C1 is

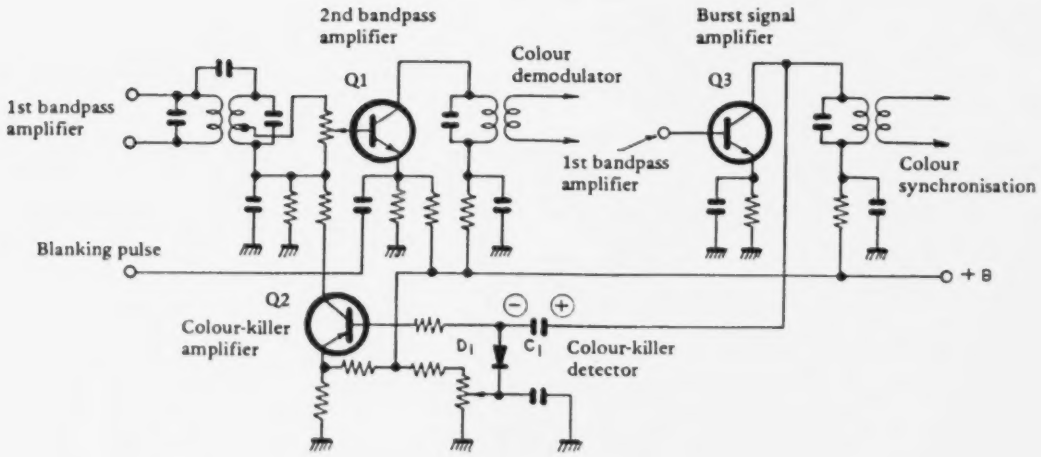


Figure 4-7(a)
Colour-killer circuit by a diode

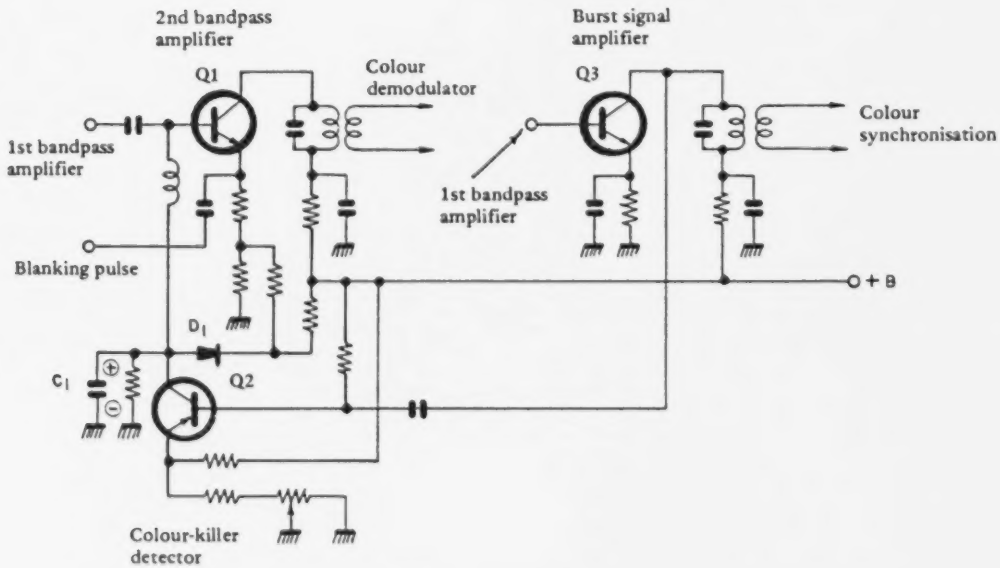


Figure 4-7(b)
Colour-killer circuit by a transistor

charged. The stored voltage across C1 triggers on Q2. When Q2 conducts, the base voltage of Q1 increases and turns on Q1. Without the burst signals the second bandpass amplifer transistor Q1 remains cut off.

Figure 4-7(b) shows a colour-killer circuit using a transistor detector. If burst signals are present, the detector transistor Q2 conducts during the negative half-cycles and C1 is charged. The stored charge or voltage across C1 will trigger the second bandpass amplifier transistor Q1. Thus when the burst signals are present, the bandpass amplifier is enabled. The diode (D1) connected to the collector of Q2 is a clamping diode. It conducts when the voltage across C1 exceeds a predetermined value and prevents Q1 from saturating.

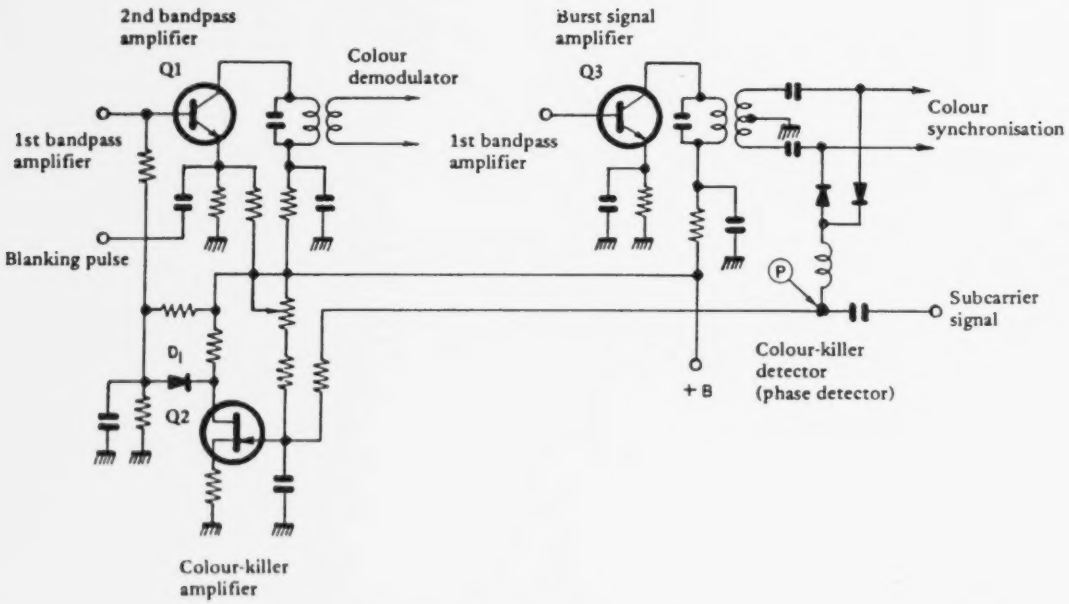


Figure 4-7(c)
Colour-killer circuit by a phase detector

Figure 4-7(c) is a colour-killer circuit using a phase-detector circuit. A FET is used to control the second bandpass amplifier circuit. The phase-detector circuit operates like the ACC phase-detector circuit. The output voltage of the detector (taken at node [P]) decreases when the burst signal is present. The output voltage is supplied to the gate of an N-channel FET (Q2). The drain current of this type of FET decreases when the gate voltage decreases. When the burst signal is present, the gate voltage as well as the drain current of Q2 decreases. When the drain current of Q2 decreases, the drain voltage increases, and this turns on the second bandpass amplifier transistor Q1. When the burst signals are absent, the second bandpass amplifier remains cut off. Thus the bandpass amplifier circuit is disabled during monochrome transmission and is enabled during colour transmission.

The diode (D1) connected to the drain circuit of the FET (Q2) conducts when the drain voltage of the FET becomes low, and it firmly disables the second bandpass amplifier transistor.

The blanking pulses are supplied to the emitter circuit of Q1 in the circuits shown in (a), (b) and (c). These pulses disable the second bandpass amplifier circuit during the horizontal retrace periods to prevent the burst signals from affecting the DC restoration of the colour-subtraction signal.

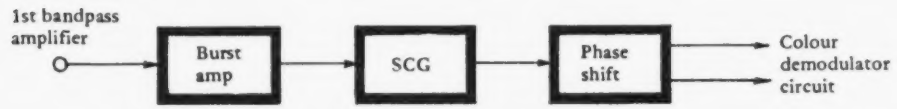
Colour synchronisation circuit

Function of the colour synchronisation circuit

Figure 4-8 shows a functional block diagram of the colour sync circuit. The main function of the colour sync circuit is to produce subcarrier signals needed in demodulating the colour signal.

The colour sync circuit uses the burst signals superimposed on the back porch of every horizontal blanking pulse to generate the subcarrier signal. A crystal with a frequency of 3.579545 MHz is used to produce a steady oscillation of the subcarrier signal.

The other functions of the chroma sync circuit are discussed in the following paragraphs.



SCG: Subcarrier signal generator circuit

Figure 4-8
Functional block diagram of a colour sync circuit

Variable hue adjustment. The colour hue, or tint, of the image should be variable to allow the viewer to adjust the tint. The hue can be controlled by changing the phase between the subcarrier and the chroma signals.

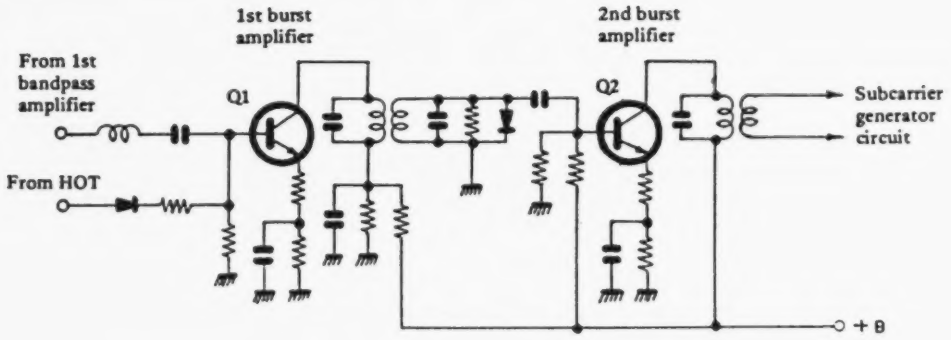
There are two ways of changing the phase relation of the chroma and subcarrier signals. One is to vary the phase of the chroma signal while keeping the phase of the subcarrier fixed. The other is to vary the phase of the subcarrier signal while keeping the phase of the chroma signal fixed. In the latter case, the phase of the subcarrier signal must be controlled within the colour sync circuit.

Generation of two or three subcarrier signals. The two-axis colour-demodulator circuit requires two kinds of subcarrier signals; the three-axis colour-demodulator circuit, three to demodulate the chroma signal. The phase of the subcarrier signals must meet the requirements of the demodulator circuit. A phase-shift circuit is used to shift the phase of the subcarrier signals to meet the phase requirements of the colour-demodulator circuit.

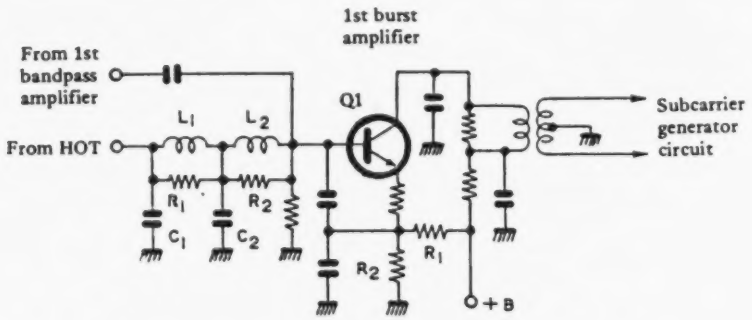
Burst signal amplifier circuit

The chroma signal amplified by the first bandpass amplifier circuit is supplied to the burst signal amplifier circuit. Then the burst signal amplifier circuit separates the burst signals from the chroma signal and amplifies them. Figure 4-9 shows examples of burst signal amplifier circuits.

In the circuit shown in (a), positive flyback pulses from the horizontal output transformer (HOT) are supplied to the burst signal amplifier transistor Q1, which is biased in cut-off. These pulses trigger the transistor on during the horizontal retrace periods. Since only the burst signals are present during the retrace



(a) Burst signal amplifier circuit using pulses from horizontal amplifier circuit



(b) Burst signal amplifier circuit using synchronising pulses

Figure 4-9
Burst signal amplifier circuits

periods, they are separated from the chroma signal and amplified.

Figure 4-9(b) shows another example of a burst signal amplifier circuit. Positive horizontal sync signals are supplied to the base of the burst signal amplifier transistor Q1. These signals are used for triggering Q1. However, the burst signals are located on the back porch of every horizontal blanking signal. Thus the horizontal sync signal has to be delayed to trigger Q1 on during the burst signal periods. The delay circuit is formed by C1, C2, L1, L2, R1 and R2.

Subcarrier signal generator circuit

Figure 4-10 shows block diagrams of subcarrier generator circuits. There are three types of subcarrier signal generator circuits: (1) crystal filter (ringing type), (2) burst signal injection lock and (3) APC (automatic phase control). All of these circuits use a crystal for a stable oscillation.

Crystal oscillator When pressure or tension is applied across a thin piece of crystal, electricity is generated at the surface. A crystal can be made to oscillate by applying an AC voltage across it through electrode plates attached at opposite surfaces of a thin piece of crystal. The oscillation of the crystal is stable and not affected by temperature changes. A crystal can be used in an electric circuit for

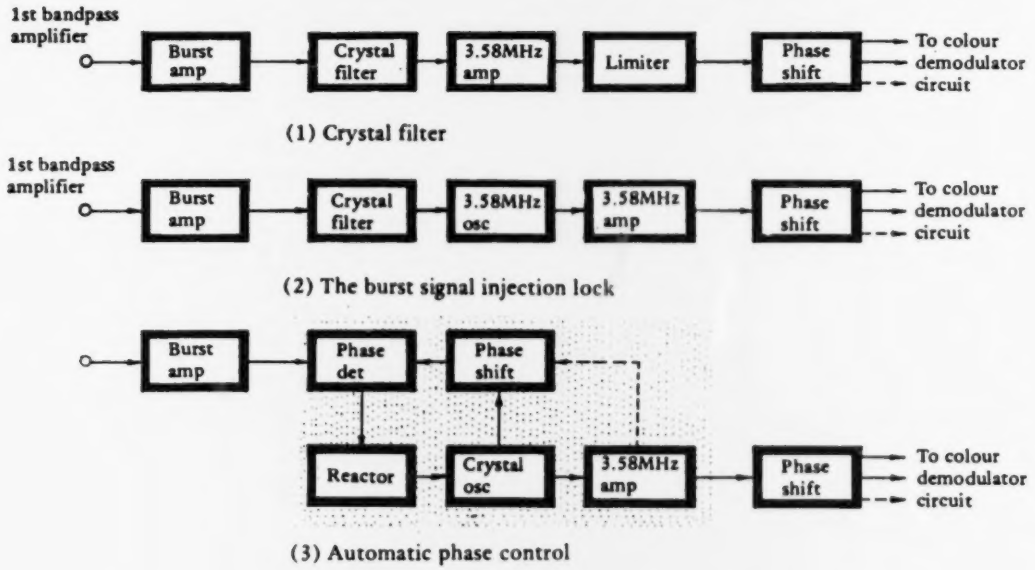


Figure 4-10
Subcarrier signal generator circuit

a steady and constant oscillation in an oscillator or filter circuit.

In Figure 4-11(a) if the magnitude of the RF voltage applied to the crystal is kept constant while the frequency is varied, the relation between the frequency of the applied voltage and the current through the crystal is shown in (c).

In (c) the frequency at which maximum current flows is called the series resonant frequency (fs), and the frequency at which minimum current flows is called the parallel resonant frequency (fp). The difference between fs and fp is very small, thus the curve at (c) can be approximated by the curve at (d). The series and parallel resonance characteristic of the crystal makes it a mechanical oscillator. Figure 4-11(b) is an equivalent circuit of a crystal. Rs, Ls and Cs are the equivalent series impedances of the crystal; Cp is the equivalent capacitance across the crystal due to the electrodes. Picture 4-1 shows crystals used as oscillators in TV receivers.

Picture 4-1
Crystals used as oscillators in TV receivers

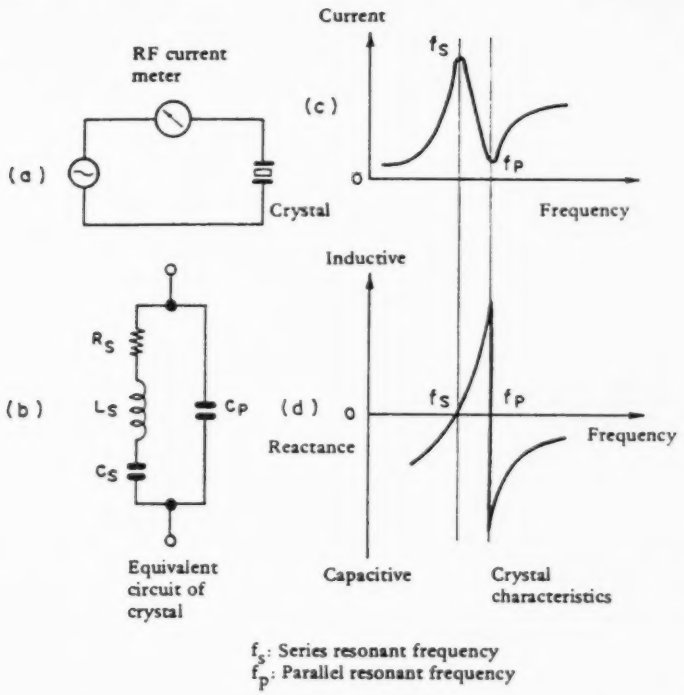


Figure 4-11
Equivalent circuit and characteristic of a crystal

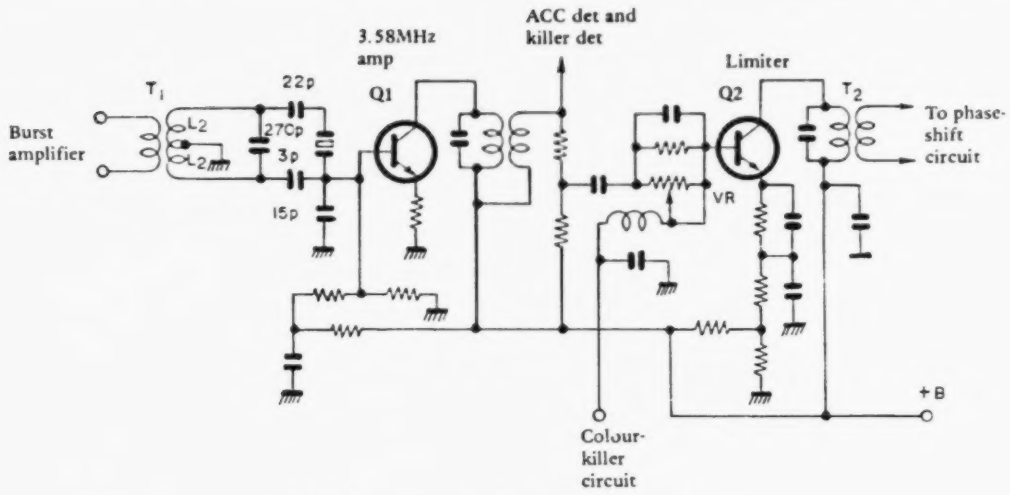
Crystal-filter (ringing type) oscillator. Figure 4-12(a) shows a subcarrier generator circuit using a crystal-filter circuit. Q1 couples the burst signals to the crystal-filter circuit, which converts them into a continuous signal. The magnitude of the continuous signal is made constant by an amplitude limiter circuit to produce a subcarrier signal. Figure 4-13(a) shows the stages in transforming the burst signals into a colour subcarrier signal.

The function of the crystal-filter circuit is explained in Figures 4-12(b) and (c). In Figures 4-12(b) and (c) the burst signals are supplied to L1 and L2 through terminals A and B. The output of the circuit is taken across terminals C and D.

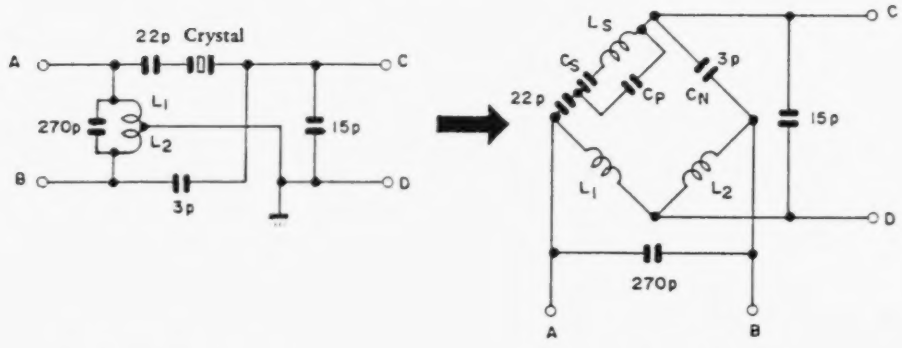
Figure 4-12(c) shows a bridge-circuit equivalent of (b). This circuit is balanced at frequencies other than the resonant frequency of the crystal filter. For a balanced bridge circuit, the formula below is satisfied.

$$CP / CN = L1 / L2$$

When the bridge circuit is balanced, the output is zero. Thus, when the frequencies of input signals and noise are unequal to the resonant frequency (fs), the output signal is zero. The crystal used in this circuit is a 3.579545 MHz crystal. When the burst signals are supplied to terminals A and B, the circuit becomes unbalanced and a continuous signal with frequency equal to the burst signal frequency is taken across C and D. Thus this filter circuit prevents interference from external signals.



(a) Crystal-filter circuit used in an actual circuit



(b) Crystal-filter circuit

(c) Equivalent circuit

Figure 4-12
Crystal-filter circuits

The variable resistor VR in Figure 4-12(a) is for the hue adjustment. The phase of the subcarrier signal is varied by around +/- 30 degrees by changing the input static capacitance of the limiter transistor Q2 through the adjustment of VR. Q2 is disabled by the colour-killer circuit during black-and-white reception

Burst signal injection lock type. Figure 4-14 shows a burst signal injection lock circuit. In the figure the 3.58 MHz oscillator circuit is autodyned and uses no crystal oscillator to generate the subcarrier signal. Instead, an accurate 3.58 MHz signal taken from the output of the crystal filter circuit is fed to the 3.58 MHz oscillator circuit. The output of the crystal filter synchronises the oscillation frequency of the 3.58 MHz oscillator circuit with the burst signals.

Automatic phase control (APC). The principle of this circuit is entirely different from the subcarrier generators. A block diagram of the circuit is shown in Figure 4-10(c). The circuit compares the phase of burst signals and the 3.58 MHz oscillator signal and produces a subcarrier signal synchronised with the burst signals.

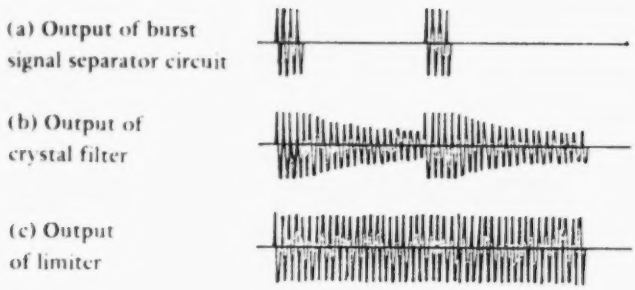


Figure 4-13
Wave-form analysis of crystal-filter circuit

Figure 4-15 shows an APC circuit. The burst signals and the output of the 3.58 MHz crystal oscillator signal (actually horizontal output pulses) are supplied to the phase-detector circuit. The phase detector determines any phase difference between the two signals and produces a control voltage which is taken out at node (P). The control voltage is supplied to the oscillator circuit and varies the voltage across the varicap diode connected in series with the crystal. The phase and the frequency of the oscillator signal are controlled by the varicap and are synchronised with the burst signals.

The APC subcarrier oscillator circuit is commonly used in colour IC TV receivers because it is reliable.

Phase locked loop (PLL). This loop belongs to the group of the APC type but uses no capacitors or inductors in the tuning circuit.

A functional block diagram of a PLL circuit is shown in Figure 4-16. It consists of a phase detector, a low-pass filter and a voltage-control oscillator (VCO) circuit. The burst signals and the output of the VCO circuit are fed to the phase-detector circuit. The phase-detector circuit compares the phase of the two signals and produces a control voltage proportional to the difference. The con-

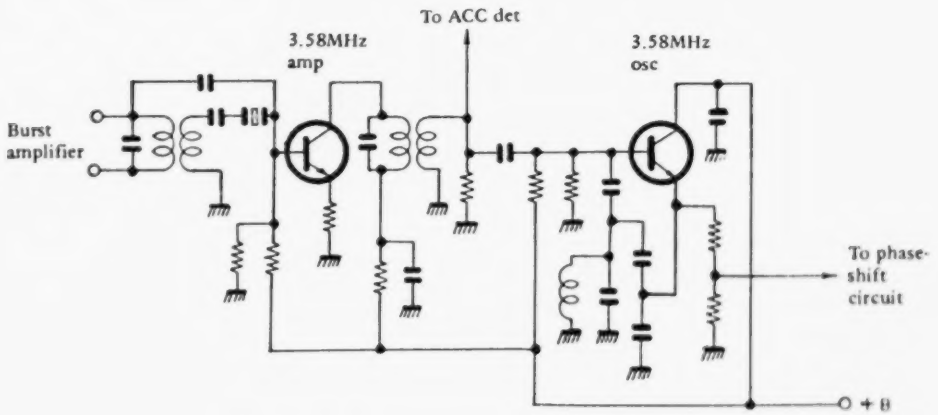


Figure 4-14
A burst signal injection lock circuit

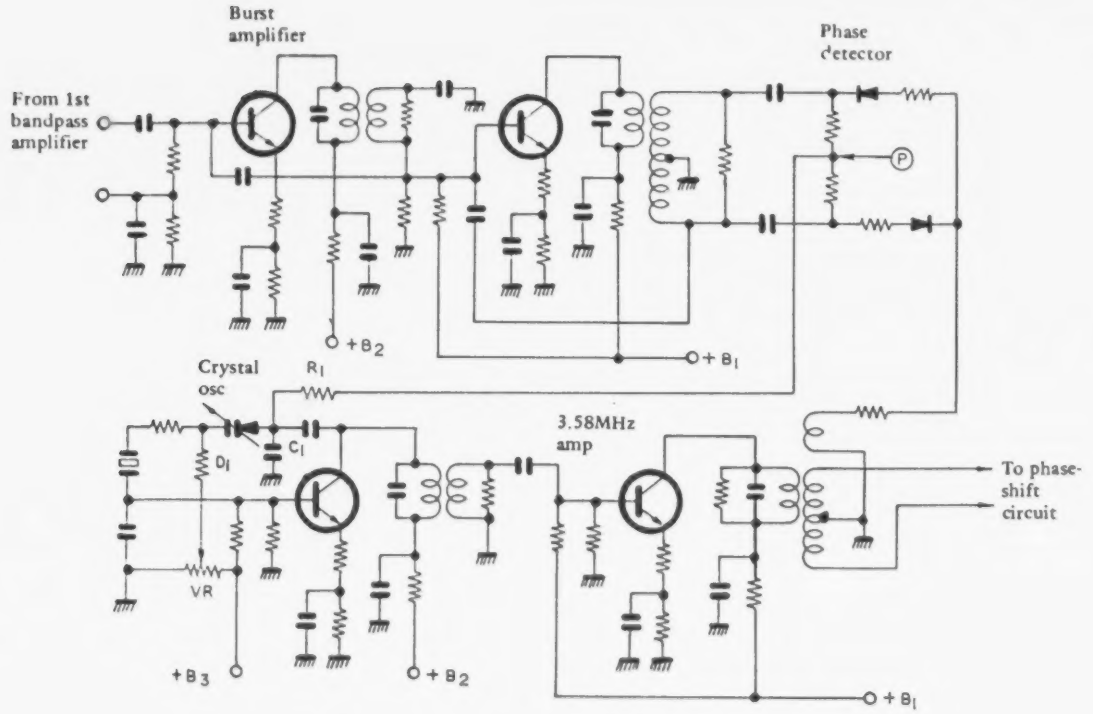


Figure 4-15
An APC circuit

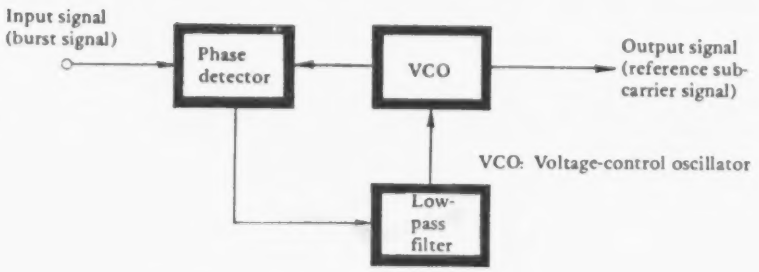


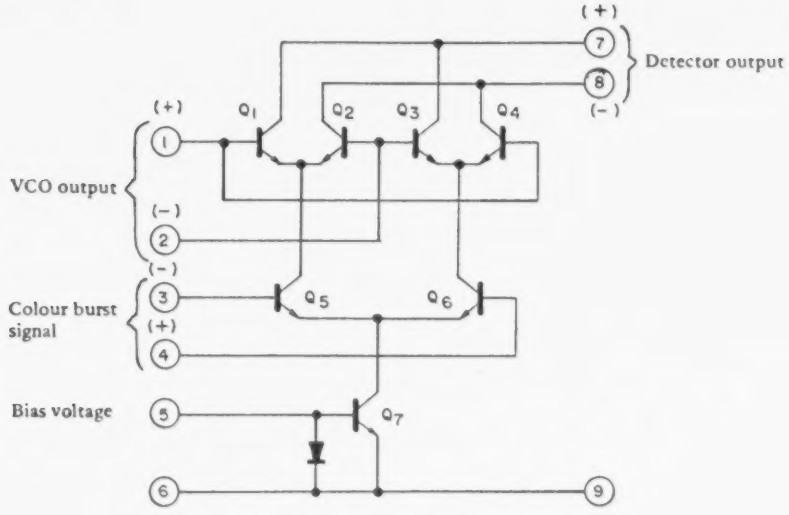
Figure 4-16
A PLL circuit

trol voltage is fed to the VCO circuit through a low-pass filter and synchronises the VCO output with the burst signals.

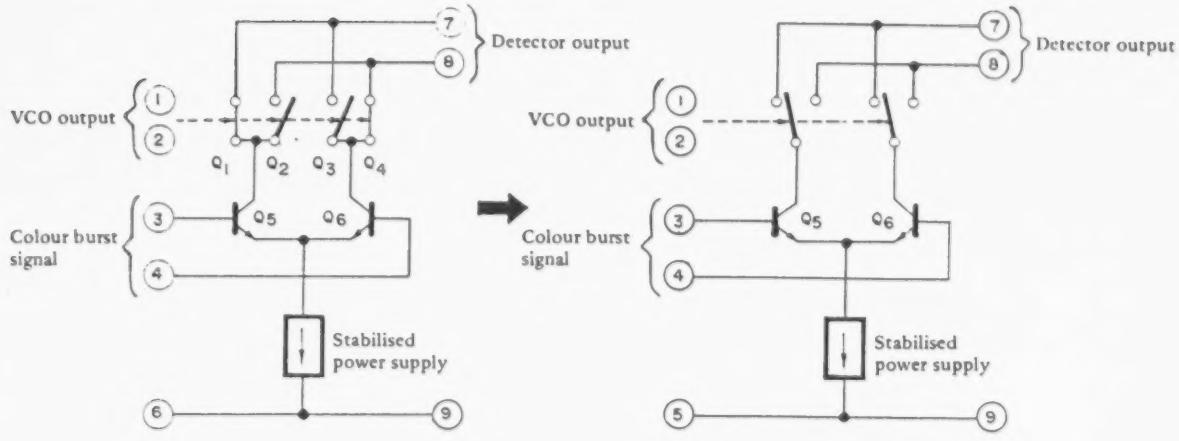
Phase-detector circuit. Figure 4-17(a) shows a phase-detector circuit. A differential amplifier circuit, dual-balanced, is usually used as a phase detector.

The output signal of the VCO is fed to the upper differential amplifiers through terminals (1) and (2); the burst signals, to the lower differential amplifier through terminals (3) and (4).

The upper differential amplifiers formed by Q1 to Q4 merely function as a switch controlled by the VCO output, as shown in Figure 4-17(b). The lower



(a) Cross collector coupling



(b) Switching of Q1, Q2, Q3, Q4 by VCO signals

Figure 4-17
A PLL phase-detector circuit

differential amplifier increases the burst signals. The amplified burst signals are alternately switched from terminals (7) to (8) by the upper differential transistors. The state of the switches (Q1 to Q4) depends on the cycle of the VCO output. The output of the phase detector depends on the phase relation between the VCO output signal and the burst signals.

Figure 4-18 shows examples of the phase-detector output for three phase relations between the VCO output and the burst signals. The examples given are for cases when the burst signals and the VCO output are 0 degrees (in phase), 180 degrees (negative phase) and 90 degrees apart. When the burst and the VCO

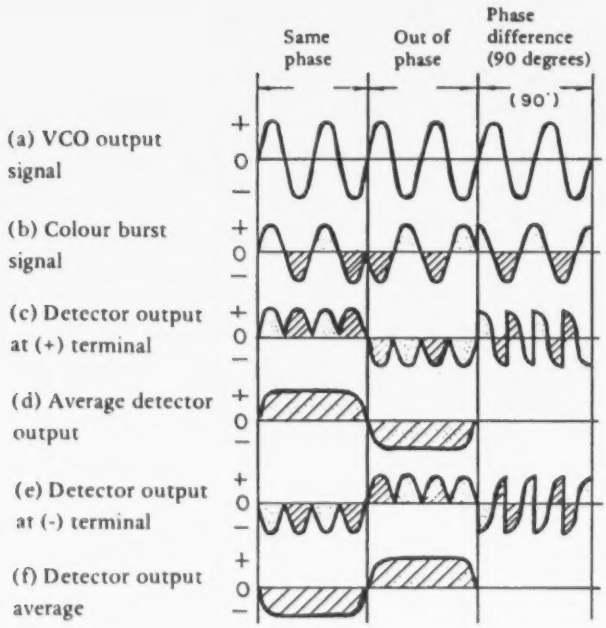


Figure 4-18
Phase relation and output voltage

signals are 0 degrees and 180 degrees apart, the average phase detector output is maximum. When the signals are 90 degrees apart, the output is zero.

VCO circuit. In inductive-coupling circuits it is impractical to use variable resistors and inductors to change the level and the phase of a signal, respectively. Instead the supply voltages of the transistors within the IC are varied to control the level and the phase of the signals.

Since the function of the IC is controlled by the supply voltage, reactive interference from other circuits can be reduced. This kind of circuit control is called voltage control. It is also used in the frequency-control circuit of the 3.58 MHz oscillator circuit of the colour sync circuit.

Figure 4-19 shows a functional block diagram of the VCO circuit. The oscillator frequency is controlled by the DC voltage supplied to the phase-shift cir-

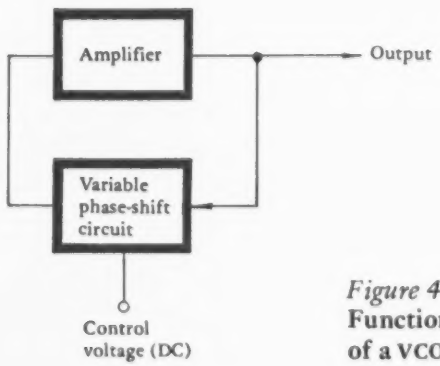


Figure 4-19
Functional block diagram of a VCO circuit

cuit. This circuit changes the phase of the feedback circuit, thus maintaining the frequency of the oscillator.

Figure 4-20 shows an actual VCO circuit. Transistors Q1 to Q6 form dual-balanced differential amplifier circuits. The output signals are independently taken out from the emitter circuits of Q7 and Q8 through R and C and then mixed together. After mixing, the output signals are fed back to the differential amplifier circuit through a crystal. The VCO circuit works like a CR oscillator circuit.

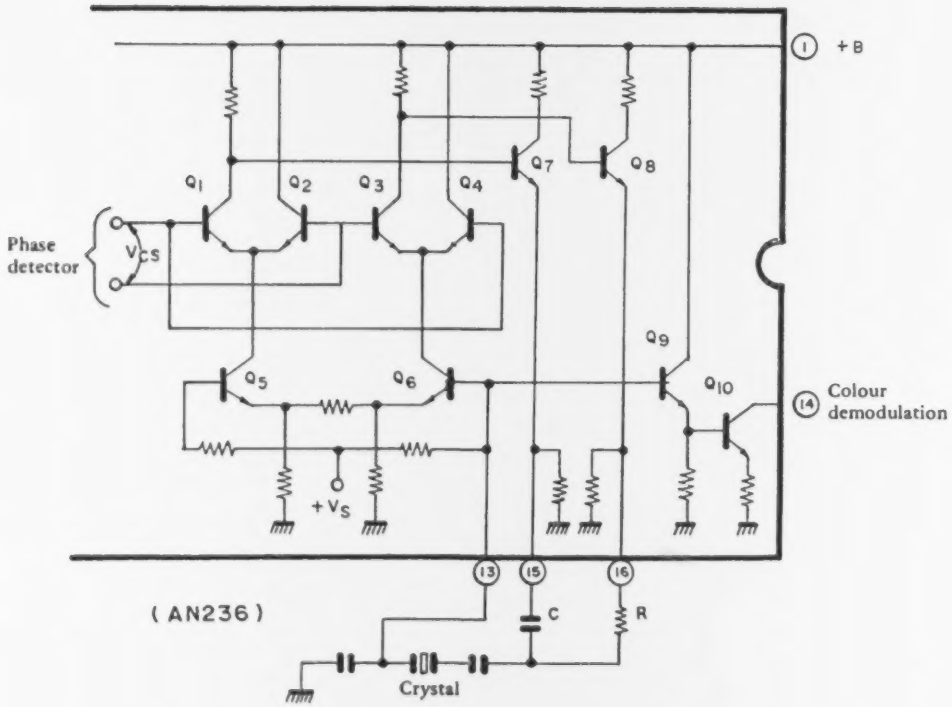


Figure 4-20
A VCO circuit

The DC voltage-control signal (VCs) produced by the phase-detector circuit is supplied to the base of transistors Q1 to Q4. This DC voltage varies the operation of the transistors. Transistors Q1 to Q4 form pairs of differential amplifier circuits, so when Q1 and Q4 conduct more, Q2 and Q3 conduct less.

If the output of Q1 increases, the signal through Q7 and C increases. On the other hand, Q3 conducts less and the signal through Q8 and R decreases. Thus the phase of the feedback signal in the feedback circuit of the VCO circuit advances (the oscillation frequency increases).

Similarly, if the output of Q1 decreases, the signal through Q7 and C decreases and the signal through Q8 and R increases. This results in a lag in the phase of the feedback signal in the feedback circuit of the VCO circuit (oscillation frequency decreases). Therefore, by supplying a DC-control voltage to the base of Q1 to Q4, the phase of the feedback signal of the VCO circuit is varied, and so the oscillation frequency of the VCO circuit is maintained.

The chroma-signal demodulation circuit

The chroma-signal demodulation circuit processes the chroma signal to produce the colour-subtraction signals.

Principle of demodulation

Generation of DSB (double sideband) signal. The chroma signal is an amplitude-modulated signal transmitted with its carrier suppressed at the transmitter. The transmitter sends only the upper and lower sidebands. This is called double sideband transmission.

Figure 4-21(a) shows a DSB generator circuit. The modulating signal is supplied to terminals A and B, the carrier signal to terminals E and F. The amplitude of the carrier signal is made greater than that of the modulating signal.

When the modulating signal alone is supplied. The signal induced at the secondary of the input transformer T1 by the modulating signal is shorted by diodes D1, D3 or D2, D4. The impedance of the output transformer T2 is much lower than the modulating signal, since the modulating signal has a frequency much lower than the frequency of the carrier signal. Thus no output is developed across terminals C and D.

When the carrier signal alone is supplied. The diodes are switched by the polarity of the carrier signal supplied to terminals E and F.

When terminal E is positive and F is negative, diodes D1 and D4 are supplied with forward bias and conduct, while D2 and D3 are reverse-biased and cut off. When the polarity of the terminals is reversed, the state of

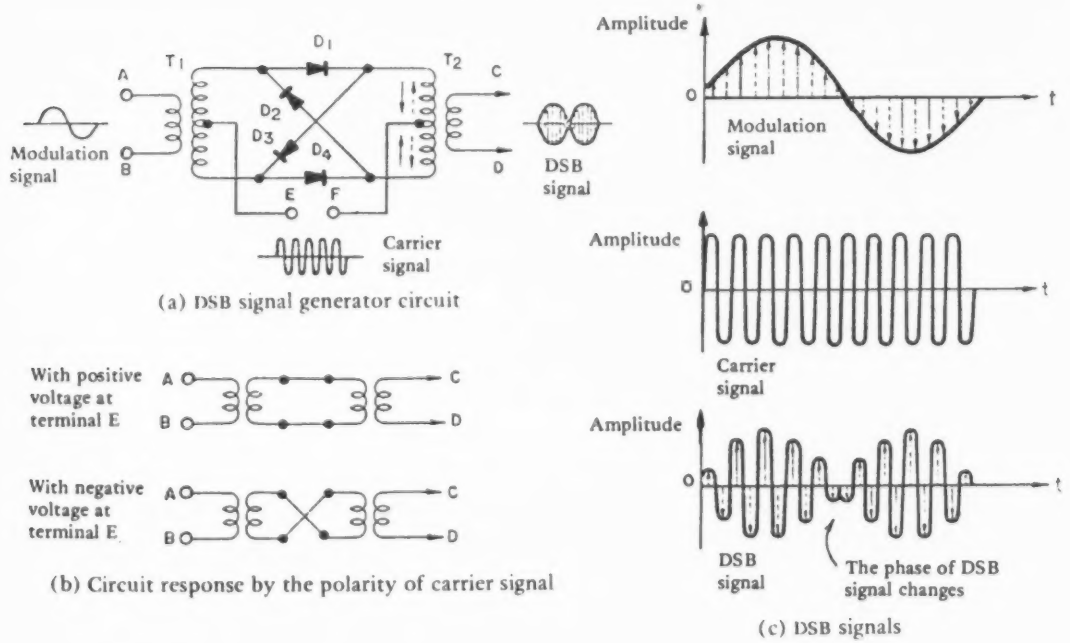


Figure 4-21
Principle of DSB signal generator circuit

the diodes is also reversed. Thus D1 D4 and D2 D3 are alternately switched by the carrier signal in every half-cycle. The currents through the primary of the output transformer T2 are equal in magnitude and opposite in direction, as shown in Figure 4-21(a). Thus the currents cancel each other out and no signal is produced across the output terminals C and D.

When the modulating and carrier signals are supplied together. In Figure 4-21 the diodes act as switches triggered by the carrier signal. Figure (b) shows how the circuit in (a) is switched by the carrier signal. As shown in (c), the modulated signal flows in opposite directions within the secondary of the output transformer T2 with respect to the cycle of the carrier signal. The signal at the output (across terminals C and D) is a signal without a carrier component but has a frequency equal to the carrier signal frequency. The amplitude of the output signal is proportional to the amplitude of the modulating signal. This kind of signal is called a DSB (double sideband) signal.

Figure 4-21(c) shows a DSB signal. The output is zero if the amplitude of the modulating signal is zero. The DSB signal at the output is in phase with the carrier signal during the positive cycle of the modulating signal and is in opposite phase with the carrier signal during the negative cycle.

Demodulating the DSB signal. The same circuit shown in Figure 4-21 is used to demodulate the DSB signal. The DSB signal is supplied to terminals A and B; the carrier signal, to terminals E and F. During demodulation the circuit operates the same way during modulation. Similarly the output is taken across terminals C and D.

The carrier signal supplied to terminals E and F for demodulating the DSB signal must be in phase and equal in frequency with the modulated carrier signal at the transmitter. In colour receivers the carrier signal needed to demodulate the DSB (chroma) signal is generated by the colour sync circuit. This signal is called the subcarrier signal.

Demodulating the chroma signal The chroma signal is a mixture of two DSB signals, the ER-EY and EB-EY signals. The carriers of the ER-EY and EB-EY signals have the same frequency but have a phase difference of 90 degrees. Thus the two DSB signals (ER-EY and EB-EY) are also 90 degrees apart.

To prevent overmodulation, the ER-EY signal is modulated at a rate limit of 1/1.14 and the EB-EY signal at a rate limit of 1/2.03 at the transmitter. Figure 4-22(a) shows the phase relation of these two signals. A complete cycle of the (1/1.14) (ER-EY) and (1/2.03) (EB-EY) modulating signals is given. Figure 4-22(b) shows the sum of the two signals. This is transmitted by the TV station as the chroma signals.

Let us discuss the demodulation of the chroma signal shown in (b). Assume the colour burst signal to be 180 degrees out of phase. By calculation using the equation of the curve in (b) or by graphic analysis, the magnitude of the demodulator output is 0.49 when the phase of the subcarrier signal (fs) is 0 degrees. From (a) this magnitude corresponds to 1/2.03 times the EB-EY signal alone, since in this case the ER-EY component of the signal is zero. Thus, when the phase of the subcarrier signal is 0 degrees, the demodulator output consists only

of the EB-EY signal. Similarly, if the phase of the subcarrier signal is 90 degrees, the demodulator output consists only of the ER-EY signal.

As shown in (b), if the phase of the subcarrier is 237 degrees, the magnitude of the demodulator output is -0.99. From (a) this magnitude corresponds to the mixture of -0.27(EB-EY) and -0.72(ER-EY) signals. This represents 1.42 times the EG-EY signal.

Let us prove that the output for this case indeed represents 1.42 times the EG-EY signal. Assume that (EG-EY)' is equal to 1/1.42 times the output signal. By multiplying the output by 1/1.42, we get an equation for (EG-EY)' as given in formula 4.1.

$$(EG\text{-}EY)' = (-1/1.42)[0.72(ER\text{-}EY) + 0.27(EB\text{-}EY)] \quad \ldots . \; 4.1$$

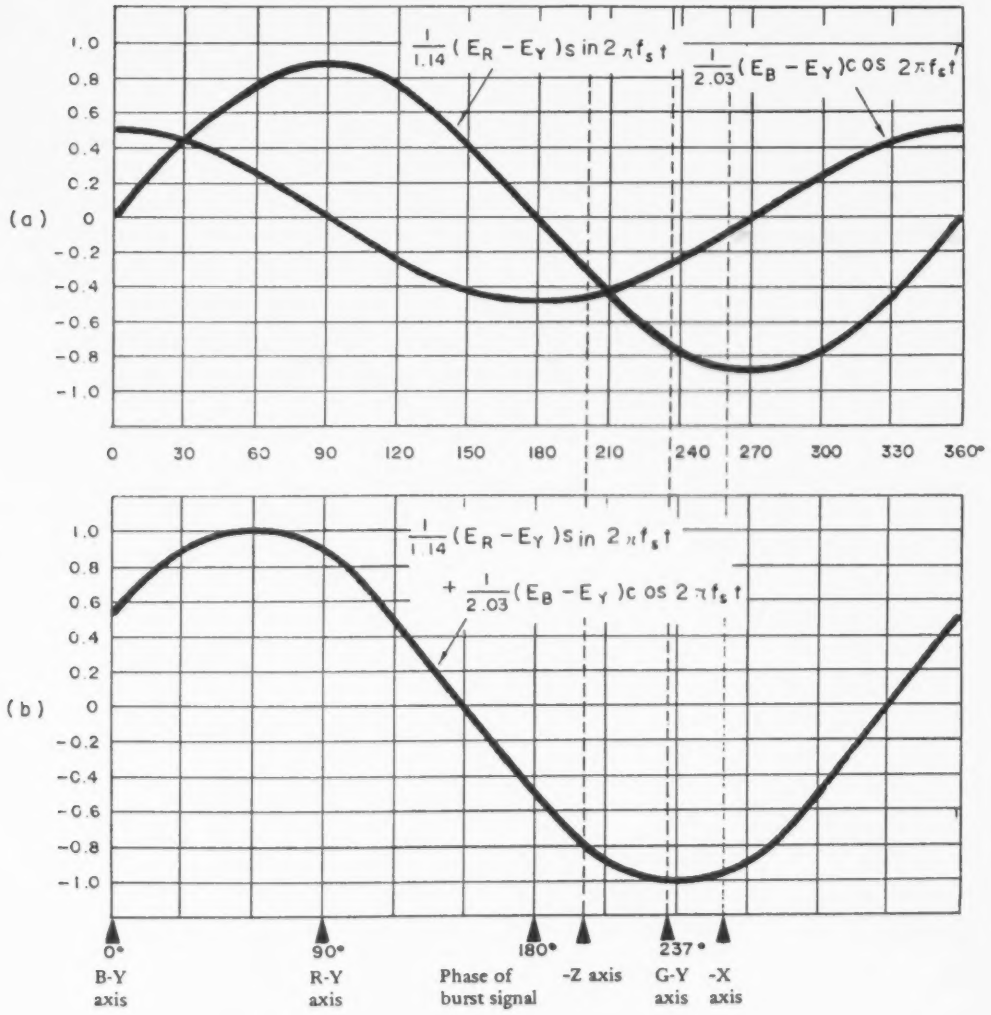


Figure 4-22
Phase shift of colour subcarrier signal and demodulation axis

To prove that (EG-EY)' is equal to EG-EY, we start with the equation for the luminance EY signal as given by

$$EY = 0.30ER + 0.59EG + 0.11EB$$

We can rewrite this equation as

$$(0.3 + 0.59 + 0.11)EY = 0.30ER + 0.59EG + 0.11EB$$

If we transfer all terms to the left and group them, we get the following equation:

$$0.3(ER\text{-}EY) + 0.59(EG\text{-}EY) + 0.11(EB\text{-}EY) = 0$$

Simplifying the equation, we arrive at the following equations:

$$EG\text{-}EY = -[0.51(ER\text{-}EY) + 0.19(EB\text{-}EY)] \ldots . 4.2$$

or,

$$EG\text{-}EY = -(1/1.42)\ [0.72(ER\text{-}EY) + 0.27(EB\text{-}EY)] \ldots . 4.3$$

We can see that formula 4.3 is equal to formula 4.1. Thus we have proved that the sum of the ER-EY and EB-EY signals at the output of the demodulator when the subcarrier has a phase angle of 237 degrees is indeed 1.42 times the EG-EY signal.

The colour-subtraction demodulation circuit where three colour-subtraction signals (ER-EY, EB-EY and EG-EY) are taken out directly from the chroma signal is called the three-axis colour-demodulator circuit. There is another kind of colour-demodulation circuit called the two-axis demodulator circuit. In the two-axis demodulator circuit, only two colour-subtraction signals (ER-EY and EB-EY) are taken out. These two signals are matrixed to form the EG-EY signal. As given by formula 4.2, the EG-EY signal is composed of 51 per cent ER-EY signal and 19 per cent EB-EY signal.

Another demodulator circuit is the XZ demodulator circuit. As shown in Figure 4-22, when the subcarrier has a phase of 260.5 and 203 degrees the EX and the EZ signals are taken at the output, respectively. Both EX and EZ signals have components of ER-EY and EB-EY signals.

The EX and EZ signals are not special colour-subtraction signals. They are simply signals having both ER-EY and EB-EY signal components. However, as shown in (a), the red signal is the major component of the EX signal; the blue, the major component of the EZ signal. 260.5 degrees and 203 degrees are chosen as the phase of the subcarrier signal because they make it easier to get the ER-EY, EB-EY and EG-EY signals in the succeeding matrix circuit. This procedure in getting the ER-EY, EB-EY and EG-EY signals is called the XZ-axis demodulation system.

Colour-subtraction signal demodulator circuits

Three-axis demodulator circuit. Figure 4-23 shows a three-axis colour-subtraction signal demodulator circuit. The circuit consists of three independent demodulation circuits supplied with their subcarrier signals. Each demodulation circuit has identical operations. Figure 4-24(a) shows a single demodulator circuit, whose equivalent circuit is shown in (b).

When the chroma signal alone is supplied. As shown in (c), the current flow in D1 and D2, respectively represented by i1 and i2, charges C opposite. Since i1 is equal to i2, the net charge across the capacitor is zero. Therefore the output is zero.

When the subcarrier signal alone is supplied. As shown in (d), the current flow in D1 and D2 charges C opposite. As in (c) the output is zero.

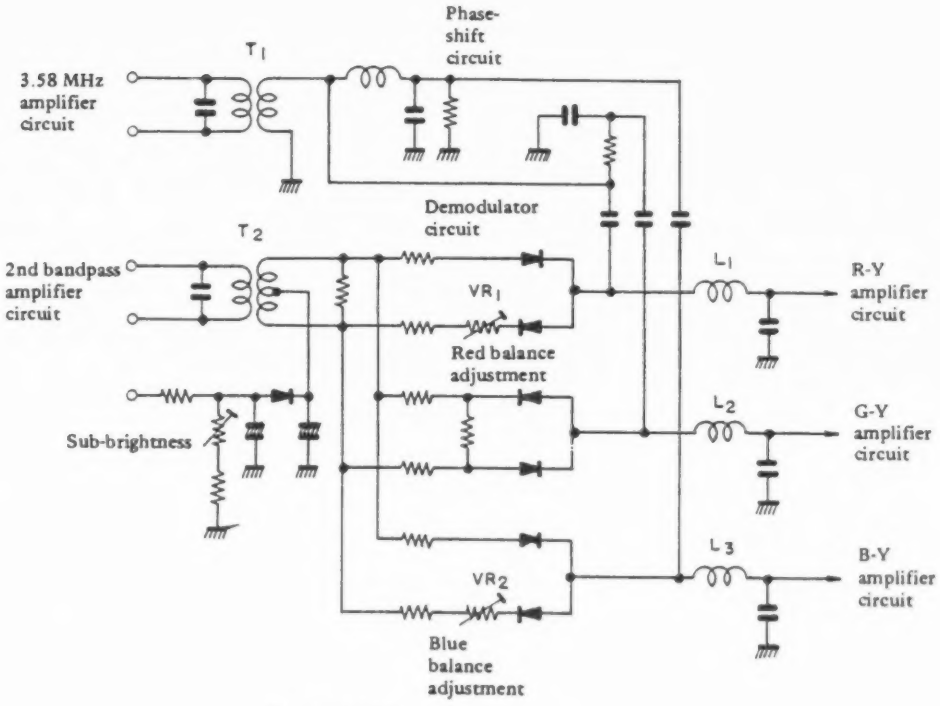


Figure 4-23
Colour-subtraction signal demodulation circuit, three-axis demodulation

When the chroma and subcarrier signals are supplied together. When the chroma and subcarrier signals are supplied to the circuit, the output voltage varies with the switching time of D1 and D2 and the polarity of the chroma signal. Figure 4-25 shows six phase relations between the chroma and the subcarrier signals for each half-cycle of the subcarrier signal. The amplitude of the subcarrier signals is greater than that of the chroma signal, making the switching of the diode dependent on the polarity of the subcarrier signal. The direction of the current flow depends on the polarity of the subcarrier signal, and the magnitude of the current

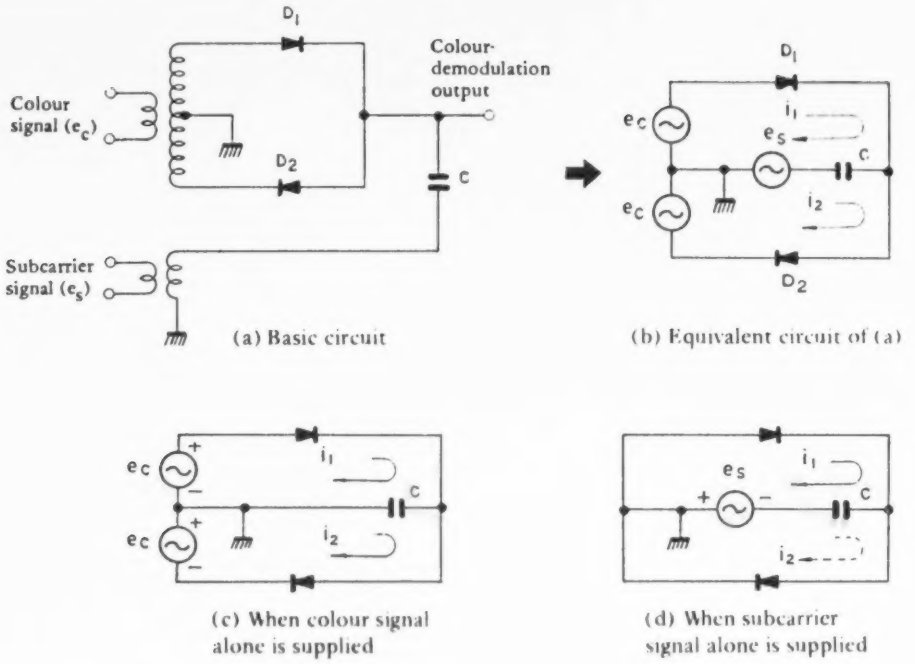


Figure 4-24
The detailed function of a colour-demodulation circuit

through the diode (also through the capacitor) is controlled by the chroma signal. The magnitude and polarity of the current flow through the capacitor for each phase relation are shown on the right side of the chart. The demodulator output is taken across the capacitor.

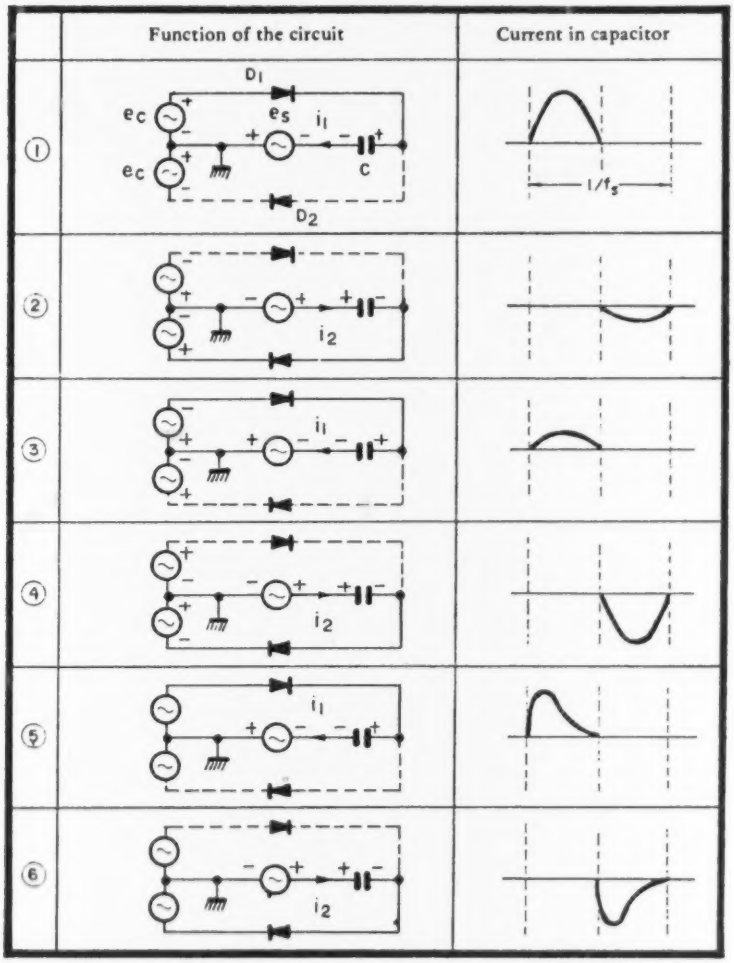
Figures 4-25(1) to (6) show every half-cycle of the subcarrier signal. Since the subcarrier signal is a sine wave, the pairs of cases (1) (2), (3) (4) and (5) (6) form one output cycle. Figure 4-26 shows few cycles in the demodulator output.

When the chroma and subcarrier signals are in phase, a large positive current flows through the capacitor during the positive cycles of the signal. In the negative cycles a small negative current flows through the capacitor. Thus the net output in one cycle of the signals is a positive voltage.

When the signals are 180 degrees apart, the net output voltage is negative, since the magnitude of the negative current exceeds the magnitude of the positive current.

As shown in Figures 4-25(5) and (6), when the phase difference between the two signals is 90 degrees, the current flow through the capacitor during the positive cycles is equal and opposite to that of the negative cycles. Thus a net negative output signal is produced. This is also the case when the phase difference between the signals is 270 degrees.

The phase of the subcarrier signals is controlled by the burst signal but remains constant in magnitude. On the other hand, the amplitude and phase of the chroma signal vary with the amount of colour in the image.



Assume the direction of i1 is positive

Figure 4-25
The phase relation of chroma and colour subcarrier signals and its output current

Therefore the output of the colour-demodulator circuit varies continuously. The output voltage becomes maximum when the two signals are in phase or 180 degrees apart. The output becomes zero when the phase difference is 90 or 270 degrees. The amplitude of the output signal varies linearly with the magnitude of the chroma signal. Figure 4-22 shows the relationship between the phase difference of the signals and the demodulator output when the amplitude of the chroma signal is kept constant.

As mentioned earlier, the chroma signal is a mixture of two DSB signals 90 degrees apart (ER-EY and EB-EY). Proper colour can be reproduced easily by selecting the phase of the subcarrier signal.

This means if a subcarrier signal with a phase exactly the same as the subcarrier signal modulated at the TV station is supplied at the demodulator circuit, the ER-EY or the EB-EY signals can be demodulated.

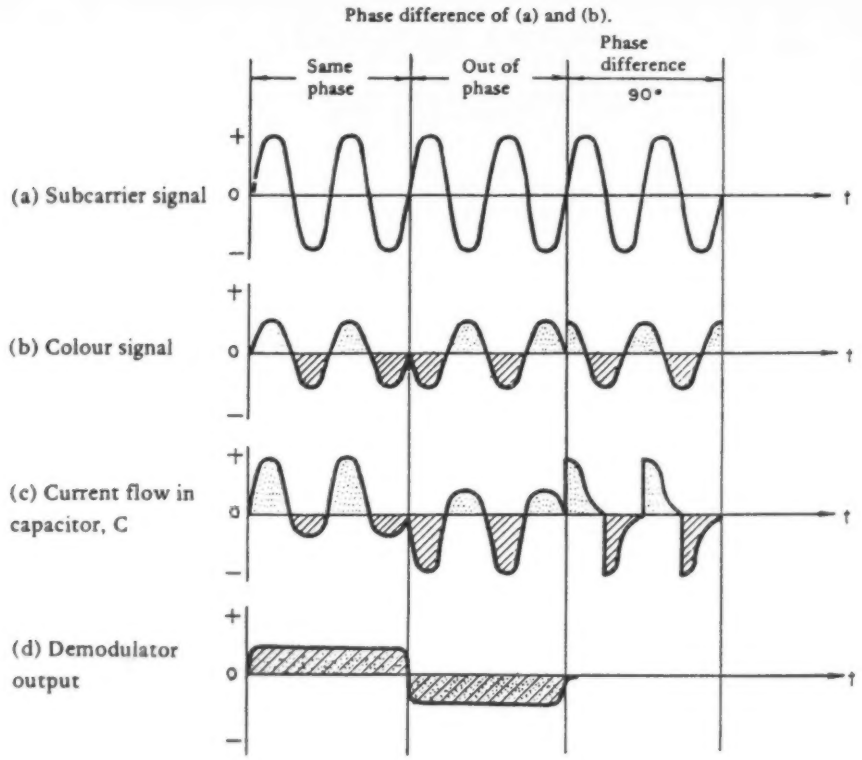


Figure 4-26
Functional wave-forms in a colour demodulation circuit

In Figure 4-23 a phase-shift circuit is used to change the phase of the subcarrier signal needed to demodulate the subtraction signals.

The red and blue adjustment controls (VR1 and VR2) will compensate for the difference in the characteristics of the diodes used as demodulators. If the diodes have no similar characteristics, the white balance (grey scale) of the raster is affected.

Two-axis demodulator circuit. Two colour-subtraction signals (ER-EY and EB-EY) are detected by the two-axis demodulator circuit. The succeeding matrix circuit develops these two colour-subtraction signals to produce the EG-EY signal. The process is done using formula 4.2. The two-axis demodulator circuit is commonly used in IC colour receivers, because the circuit becomes complicated using conventional parts.

XZ-axis demodulator circuit

Figure 4-27 shows an XZ-axis demodulator circuit. The circuit works like the two-axis demodulator circuit except when selecting the phase of the subcarrier signal. The phase of the subcarrier signal is set to a value such that the demodu-

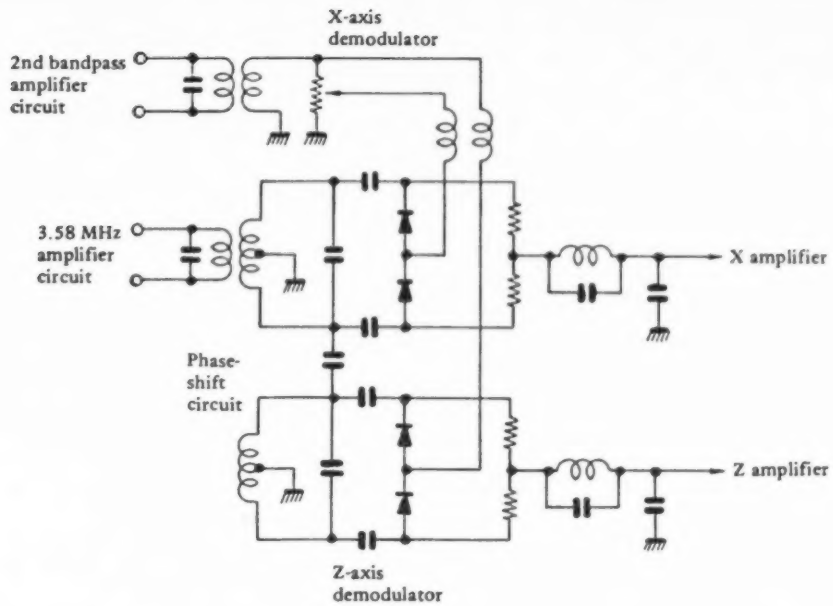


Figure 4-27
An XZ-axis demodulator circuit

lator outputs are the EX and EZ signals as discussed in the section on "Principle of Demodulation." The subcarrier signal is taken out from the B-Y axis, and the phase of the subcarrier signals is selected at 260.5 and 203 degrees for the X and Z axes, respectively.

Colour matrix and output circuit

Structure and function of the circuit

The three electron beams of the colour cathode-ray tube (CRT) must be modulated by the colour signals in order to reproduce colour image on the screen. There are two systems used in modulating the electron beam. One is called the primary-colour drive system and the other is the colour-subtraction drive system.

In the primary-colour drive system, the three colour signals (ER, EG and EB) are modulated with the luminance (EY) signal before they are supplied to the CRT. The modulated signals are usually supplied to the respective cathodes of the colour CRT.

This type is commonly used in solid-state colour TV sets. In the colour-subtraction system the colour-subtraction signals (ER-EY, EG-EY and EB-EY) and luminance signal (EY) are independently supplied to the different electrodes (first grid and cathode, respectively) of the colour CRT.

To reproduce colour images on the screen, it is necessary to supply either the three primary-colour beams modulated with the luminance signal or the colour-subtraction and luminance signals together to the colour CRT. These signals must have sufficient amplitudes to drive the colour CRT. The colour-output circuit amplifies the demodulated colour signals to a level enough to drive a colour CRT.

The output of the colour demodulator circuit is either the colour-subtraction signals or the XZ-axis signals, depending on the demodulator circuit used. These signals must be converted into either the three primary-colour signals or the colour-subtraction signals, depending on the system used in driving the CRT.

A matrix circuit converts the output of the colour-demodulator circuits into the signals required by the colour CRT drive circuit used. The function of the matrix circuit varies with the type of demodulator circuit and the drive system. The functions of the matrix circuits are summarised below.

Two-axis demodulation circuit. The matrix circuit develops the ER-EY and the EB-EY signals to form the EG-EY signal.

XZ-axis demodulation circuit. The matrix circuit forms the ER-EY, EG-EY and EB-EY signals from the EX and EZ signals.

The primary-colour drive system. The matrix circuit adds the luminance signal (EY) to the three colour-subtraction signals (ER-EY, EG-EY, EB-EY) and produces three primary-colour (ER, EG and EB) signals.

Matrix circuit of the primary-colour drive and its output circuit. Figure 4-28 shows a primary-colour drive circuit. The three colour-subtraction signals and the luminance signal are supplied to the colour-output circuit.

The colour-output transistors Q1, Q2 and Q3 are used in a common-base configuration with respect to the luminance signal and in common-emitter configuration with respect to colour-subtraction signals. The transistors develop and amplify the colour-subtraction and luminance signals to produce the three primary-colour signals to drive the colour CRT.

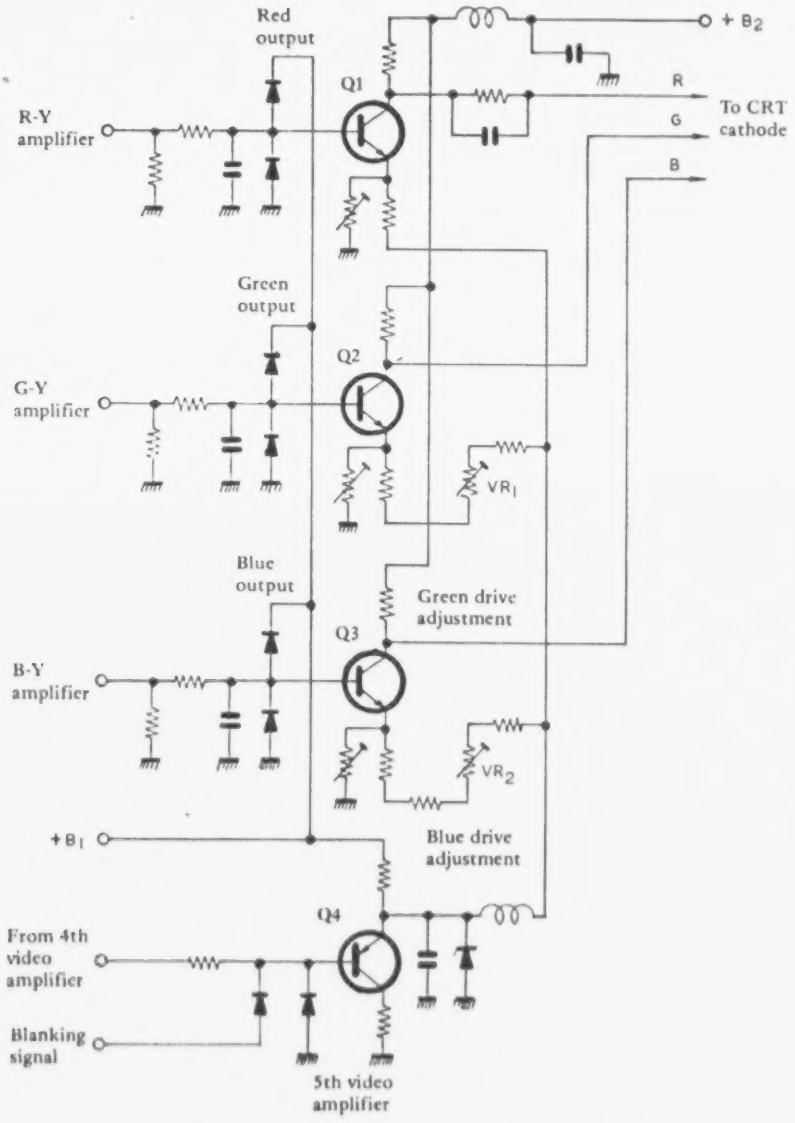


Figure 4-28
A primary-colour drive circuit

The drive-adjustment resistors VR1 and VR2 set the level of the EG-EY, EB-EY and EY signals to the proper beam ratio of the three primary colours.

Matrix circuit of the colour-subtraction drive and its output circuit

Figure 4-29 shows a colour-subtraction drive output circuit. The EX and EZ signals from the demodulator circuit are amplified by the X and Z amplifier circuits, respectively. The output circuit also functions as a matrix circuit. In principle, the base of the G-Y amplifier transistor is grounded on the signals, as shown in Figure 4-30.

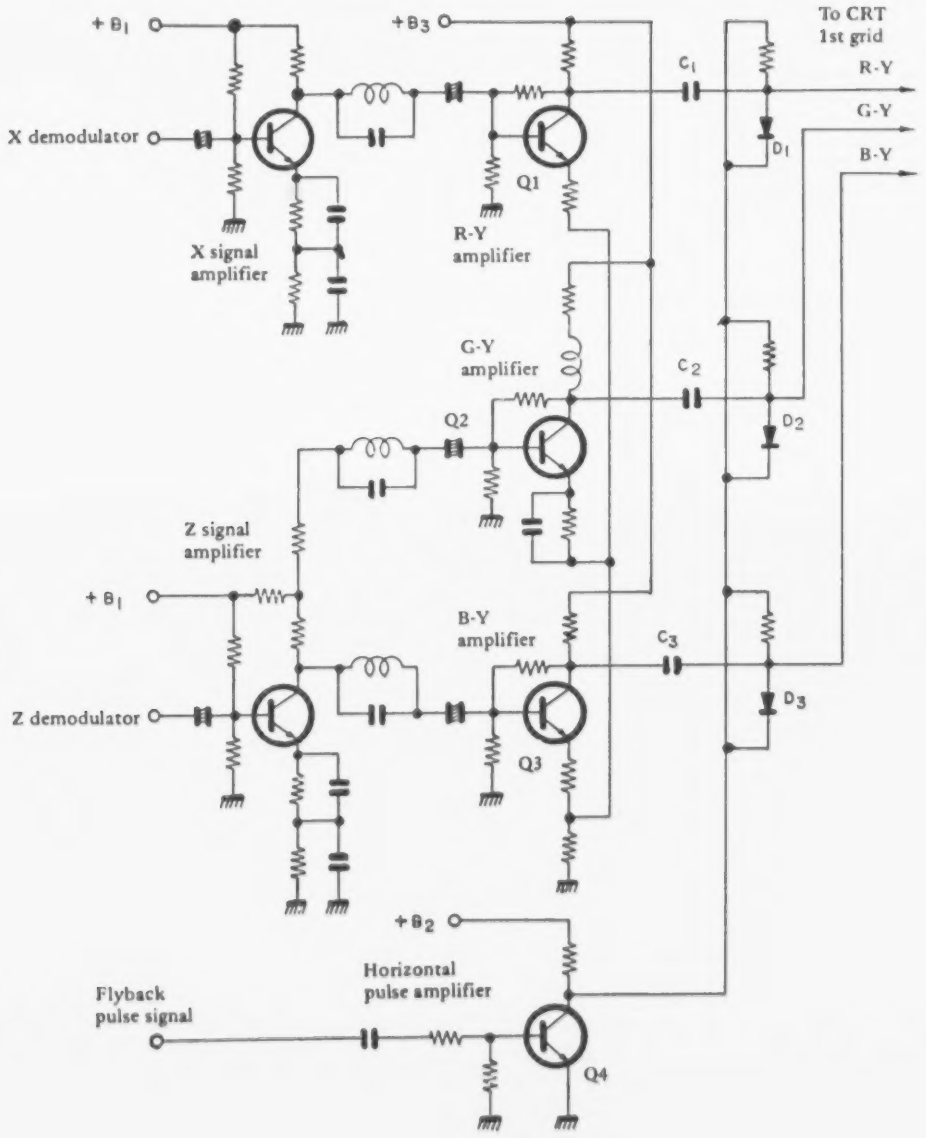


Figure 4-29
A colour-subtraction drive output circuit

In Figure 4-30, when the EX and EZ are supplied to the output transistors Q1 and Q3, a voltage is generated across the common-emitter resistor RE. This voltage is denoted by EE (Figure 4-30). Thus the base-emitter voltages (Vbe) across Q1 and Q3 are EX-EE and EZ-EE, respectively. The voltage across RE is supplied to the emitter of Q2. Therefore if the EX and EZ signals such as the EX-EE = -(ER-EY) and the EZ-EE = -(EB-EY) signals, and EE = (EG-EY) are supplied from the demodulator circuit, the three colour-subtraction signals ER-EY, EB-EY and EG-EY are obtained at the collector circuit of Q1, Q2 and Q3, respectively.

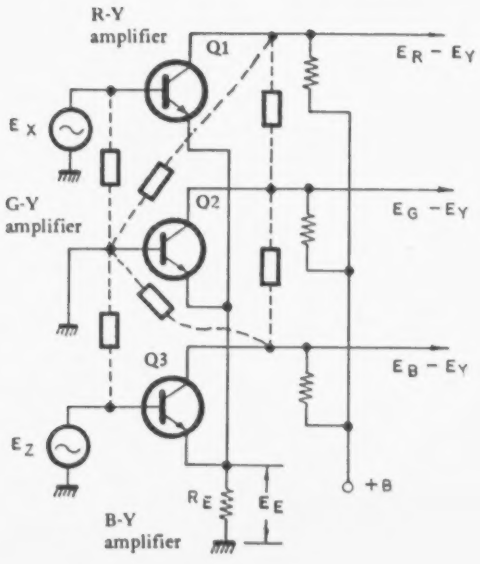


Figure 4-30
Matrix circuit made out of common-emitter circuits

DC restoration circuit

If the DC component of the colour-subtraction signals produced by the colour-demodulation circuit is not completely coupled to the colour CRT, the hue or colour of the reproduced image deviates from the original. For example, if the background colour changes, the colour of the object also changes.

In Figure 4-29 the DC component of the collector signal of the colour-output transistors is not coupled to the first grid of the colour CRT, because the collector outputs are AC-coupled to the CRT by capacitors C1 to C3. Thus colour is not properly reproduced.

Figure 4-31(a) shows part of the colour-subtraction signal output circuit in Figure 4-29. The colour-subtraction signal demodulated by the demodulator circuit is not symmetrical to the level shown in (b). This is the reference level. If this signal is capacitively coupled to the circuit shown in (c), the current flow at the positive cycle of the colour-subtraction signal charges C. When this happens, the reference level of the colour-subtraction signal is shifted by EC (voltage across the capacitor), as shown in (d). The magnitude of EC is proportional to the amplitude of the colour-subtraction signal. This voltage varies the bias of the CRT. Even if the level of the colour-subtraction signal is constant, the bias voltage of the CRT is still shifted. This makes proper colour reproduction impossible.

To get proper colour reproduction, a DC circuit is used to restore the DC component of the signal. For this purpose, the voltage stored in capacitor C is discharged during the horizontal retrace period. A switch, shown in (e), is closed during the horizontal retrace period and discharges C. When the capacitor is discharged, the colour-subtraction signal returns to its original level. Even when

the colour-subtraction signals are capacitively coupled to the CRT, the CRT is maintained at the reference level. Thus, proper colour is reproduced.

In the actual circuit shown in (a), the switch SW is replaced by D1. Q4 is keyed on by the horizontal sync pulses during the horizontal retrace periods. When Q4 conducts, the collector voltage decreases and D1 starts to conduct. When D1 conducts, C1 discharges through it. Thus the colour-subtraction signal is coupled to the CRT with the proper reference level.

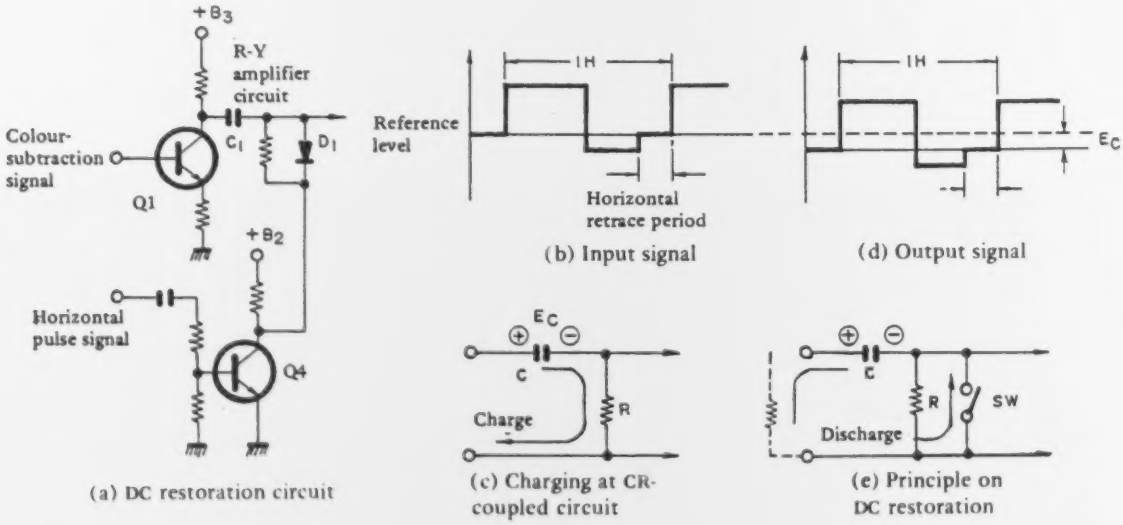


Figure 4-31
DC generator circuit and its principle

Chroma-signal processing circuit by inductive coupling (IC)

The block diagram

The IC chroma-signal demodulation circuit processes the chroma signal into the colour-subtraction signals. In modern colour TV sets this function is performed by a single IC. However, some receivers use more than one IC.

It is difficult to include capacitive and inductive components within an IC chip. To reduce discrete components, the design of the IC chroma-signal processing circuit is very different from the conventional solid-state circuit.

Figure 4-33 shows a chroma-signal processing circuit using a single IC. The principle in circuits using more than one IC is similar. Instead of an IC doing the entire operation, the function is divided among two or three ICs.

In Figure 4-32 the composite video signal which includes the chroma signal is taken out from the video pre-amplifier circuit and then fed to the bandpass amplifier circuit. Since the circuit has a narrower bandwidth and is tuned to the frequency of the chroma signal, the output consists only of the amplified chroma signal. The signal is then fed to the IC. The IC processes the chroma signal into the colour-subtraction signals (ER-EY, EG-EY and EB-EY) and then supplies them to the output transistors.

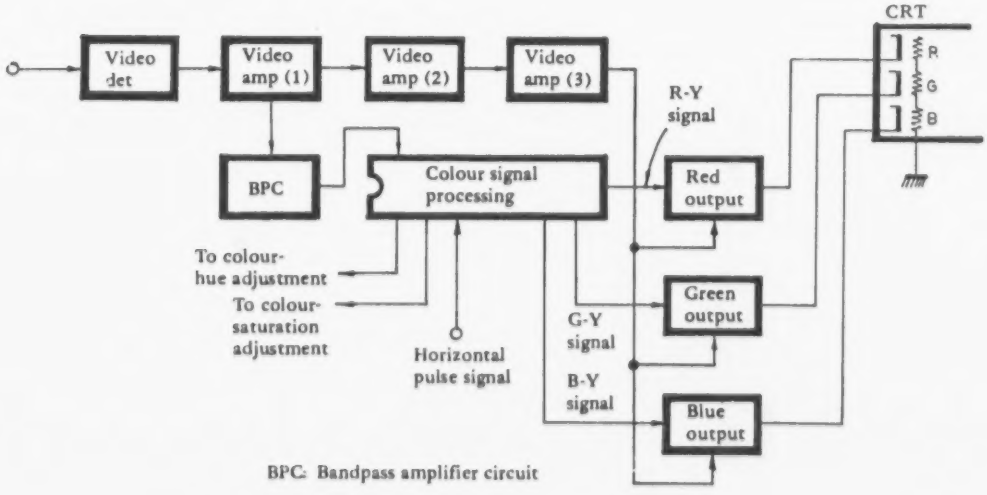


Figure 4-32
Functional block diagram of an IC colour signal processing circuit

In the block diagram shown in Figure 4-32, transistors are used for the colour-output circuit. This is because the CRT drive circuit used in the block diagram of Figure 4-32 is a primary-colour drive circuit which requires around 100 Vp-p to drive the colour CRT. An IC is not capable of handling such a high-level signal. Transistors are also used at the output to protect the IC from the internal static discharge of the colour CRT.

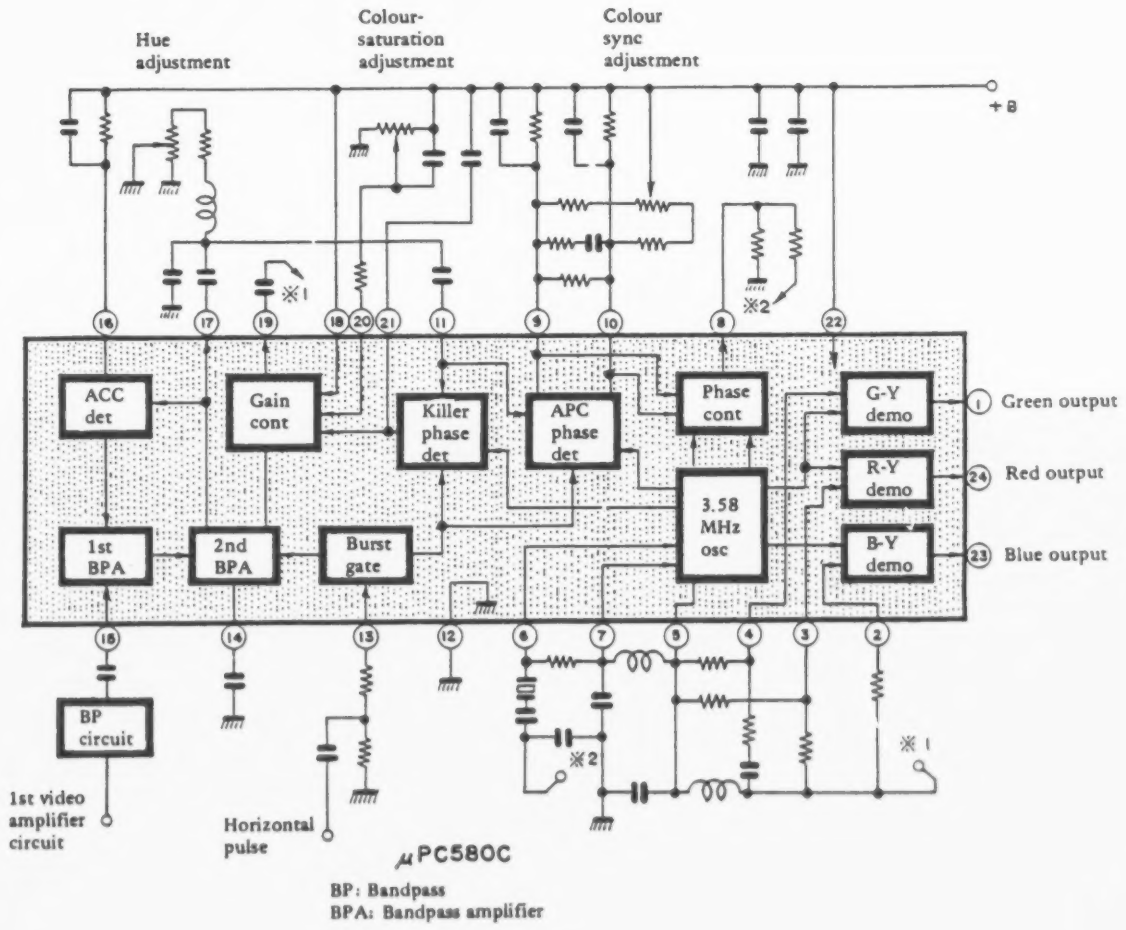


Figure 4-33
An IC colour signal processing circuit

The structure of the oscillator and detector circuit within the IC chip varies slightly with the circuits of other ICs. However, their functional block diagrams are similar.

Functional and internal block diagram of an IC used for chroma-signal reproduction

Figure 4-33 shows an internal block diagram of an IC used in the chroma-signal reproduction circuit. This IC performs the entire chroma-signal processing.

The chroma signal is fed to the input pin 15. From pin 15 the signal is fed to the gain-control circuit through the first and second bandpass circuits. The horizontal flyback pulses fed at pin 13 are used to clip the burst signal by the gate circuit. The clipped burst signal is then fed to the ACC circuit, which detects the magnitude of the burst signal to produce a DC-control voltage for the gain control of the first bandpass amplifier circuit. The burst signal is also

fed to the hue-control circuit through pin 17. The burst signal is fed back to the IC through pin 11 for the colour-killer and APC functions.

The chroma signal with the burst signal separated by the gate circuit is fed to the colour-saturation circuit. The colour-saturation-control circuit controls the magnitude of the colour and is located outside the IC. The gain-control circuit regulates the chroma signal through the colour-killer and colour-saturation adjustment. The regulated signal is taken out from pin 19 and then fed to the colour-demodulator circuits (R-Y, G-Y and B-Y) through pins 2, 3 and 4.

The subcarrier signal which is generated by the 3.58 MHz oscillator circuit is supplied to the colour-demodulator, colour-killer, APC and phase-control circuits.

The APC circuit is composed of a phase-detector circuit. It compares the phase of the burst signal from pin 11 with the phase of the subcarrier signal. When a phase difference is detected, the phase detector produces a control voltage to lock in the phase of the subcarrier to the phase of the burst signal.

The phase-detector circuit is also used by the colour-killer circuit. The absence of the burst signal is detected by the phase-detector circuit during monochrome transmission, and the colour-killer circuit is disabled by the gain-control circuit. (See Figure 4-33.)

Dynamic function of the chroma IC

Inductive couplings are purely made of semiconductor materials. The amplifiers within an IC are coupled directly. The IC is much affected by changes in the surrounding temperature and the supply voltage. To prevent changes in the IC's characteristics during operation, the power-supply circuit should be precise and the IC should operate in normal temperatures. However, as described in the section on "Subcarrier Signal Generator Circuit," the supply voltage of the IC is varied to change the level and frequency of the signal within the IC.

Figure 4-34 shows the internal circuit of an IC bandpass amplifier circuit. The chroma signal is amplified by transistors Q9, Q4, Q7, Q8 and Q13. Q1, Q2, and Q3 are used for the ACC function. The burst signal, which is proportional to the magnitude of the chroma signal, is fed to Q1 and detected. A DC voltage proportional to the magnitude of the burst signal appears across the emitter-capacitor of Q1. This DC voltage is amplified by Q2 and supplied to Q3. The collector current of Q3 changes with the magnitude of the burst signal.

Q9 functions as a current regulator. The current flowing through Q9 is the sum of the current flow through Q3 and Q4. The change in collector current of Q3 affects that of Q4. When the level of the burst signal increases, the collector current of Q3 increases while the collector current of Q4 decreases. Therefore the gain of Q4 is decreased and ACC action is performed. The ACC action is externally controlled by variable resistor VR, which varies the base voltage of Q1.

The following paragraphs further explain the circuits used within the bandpass amplifier IC shown in Figure 4-34.

Differential amplifier circuit. This circuit stabilises the operation of the IC with respect to changes in supply voltage and temperature. In Figure 4-34 the transistors Q1, Q2, Q3, Q4 and Q6 and D5 form differential amplifier circuits. Q1, Q2 and Q3 are symmetrical to Q4, D5 and Q6, respectively. They maintain

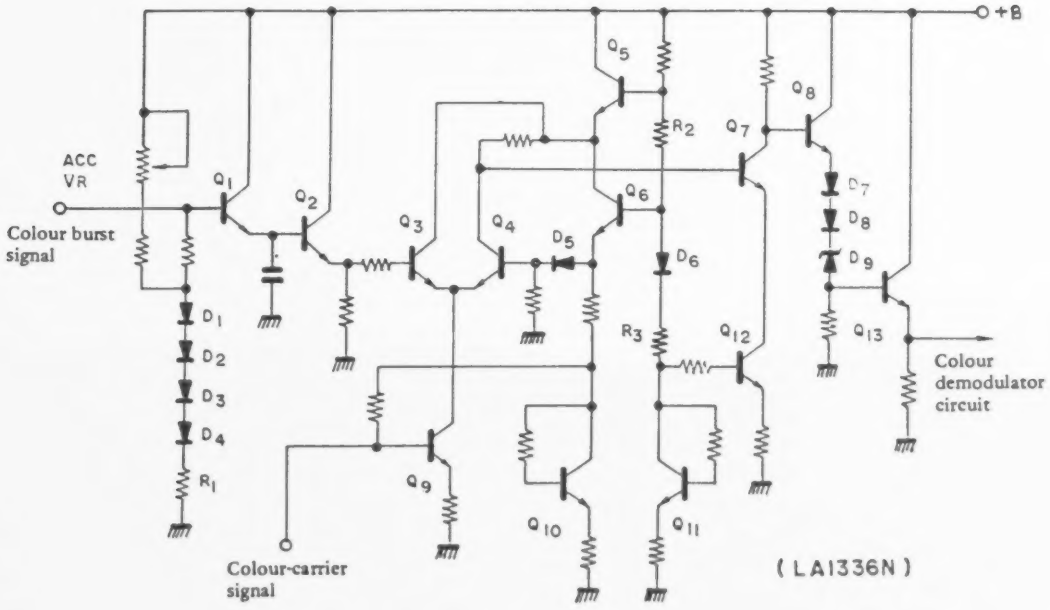


Figure 4-34
Equivalent circuit of an IC used for the bandpass amplifier circuit

the balance of the differential amplifier circuit.

Voltage regulator circuit. This circuit is formed by Q5, D6 and D11. The regulator circuit prevents the shifting of the operating point of Q7. Q11 merely functions as a diode and maintains the base voltage of Q6 together with D6 despite changes in the supply voltage temperature. When Q6 has a stable base voltage, the base voltages of Q4 and Q7 and the emitter voltage of Q6 are also stabilised.

DC level-shift circuit. Diodes D7 to D9 form a DC level-shift circuit. This circuit makes the emitter voltage of Q8 equal to the base voltage of Q13. Zener diode D9 actually sets the voltage of the DC shift level. D7 and D8 compensate for the changes in the characteristic of D9 due to changes in temperature. The voltage across D9 increases when its temperature increases. However, D7 and D8 are in series with D9. When the temperature increases, the voltage drop across D7 and D8 decreases and compensates for the voltage increase across D9. Hence the overall DC shift level is not altered.

Temperature compensation circuit. The voltage (Vbe) across the base-emitter junction of a transistor decreases with the increase in temperature. When the voltage supply to the base is kept constant, a rise in temperature will increase the base current and the collector current. An increase in the collector current changes the dynamic function of the transistor. To prevent changes in the dynamic function, a compensating circuit is used to keep the base current constant by decreasing the base voltage when the temperature increases.

In Figure 4-34, D1 to D4 compensate for the changes in the base-emitter voltages of Q1 to Q3. When the temperature rises and Vbe of the transistors decreases, the voltage between the anode and cathode of the diodes also decreases. This decrease in the voltage keeps the base current of the transistor constant. Thus the initial decrease in the base-emitter voltage is compensated. D6, Q11 and Q12 perform the same function to compensate for the changes in the voltage of Q4, D5 and Q6.

The voltage changes in the base-emitter junction of Q9 and Q12 are compensated by Q10 and Q11, respectively.

The structure of the circuit within the IC chip looks very complicated. The complication, however, is due to the compensation circuit used to stabilise the circuit's operation despite changes in temperature and supply voltage.

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